User's Manual

TYPE AJ71C24-S8

A Series
Programmable
Controllers

MITSUBISHI

Cat. No. **UMCM-(8)**

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INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.

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1. GENERAL DESCRIPTION

This User's Manual describes the specifications, handling and transmission control protocols of the AJ71C24-S8 computer link module.

The AJ71C24-S8 has one RS-232C port and one RS-422 port. It is the interface between a PC CPU and an external device (such as a computer or printer) or to the CPU of another PC station.

Dedicated transmission protocols 1 to 4 are used as transmission control procedures on the AJ71C24-S8 and a no-protocol mode and a bidirectional mode are also available. The user can select and set these independently for the RS-232C and RS-422 ports.

When using a dedicated transmission protocol or the no-protocol mode/bidirectional mode, data is transmitted using the codes as shown below.

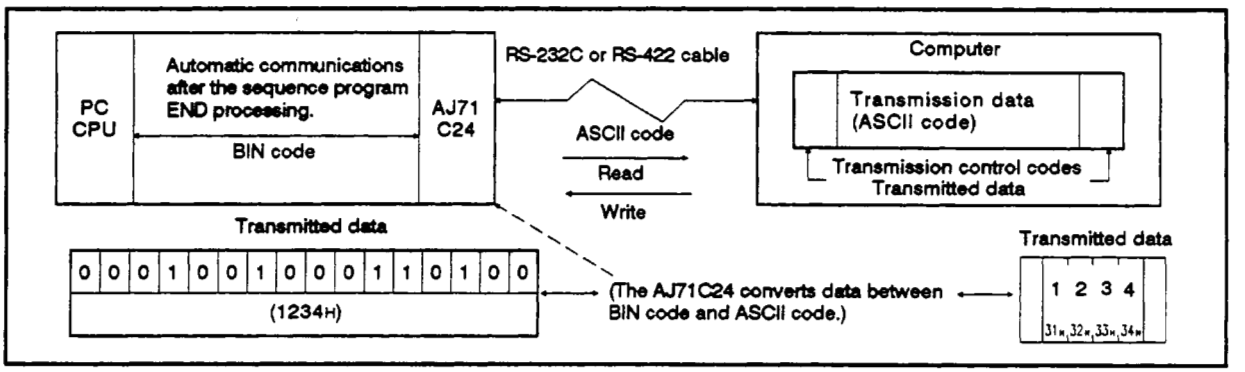


Fig. 1.1 Data Transmission with the Dedicated Protocol

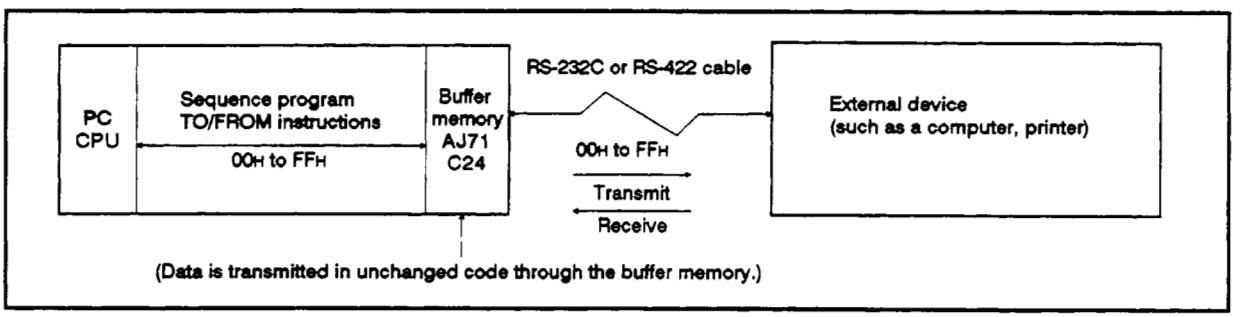


Fig. 1.2. Data Transmission in the No-Protocol Mode/Bidirectional Mode

Compared with the AJ71C24-S3 and AJ71C24-S6 computer link modules, the AJ71C24-S8 supports the following six additional functions:

(1) to (6) are the additional functions when compared with the AJ71C24-S3

(1) Commands dedicated for use with the A2ACPU(S1) and A3ACPU:

All memory devices of the A2ACPU(S1) and A3ACPU (the AnACPU in this manual) are accessible using these dedicated commands.

(2) Data transmission in the bidirectional mode:

This feature allows the AJ71C24-S8 to interface 1:1 data communications using the ACK code between a PC CPU and a computer.

When data is transmitted from the AJ71C24-S8 to a computer, a control code ENQ, the data length code, and a check sum are added respectively to the beginning, the middle, and the end of the send message. (The check sum is optional.)

When the AJ71C24-S8 receives data from a computer, it transmits a control code ACK/NAK back to the computer. This indicates the result of the receive (normal/abnormal).

The AJ71C24-S8 thus adds the ENQ code, data length, and check sum and checks the reception of the response message at the data transmission. It checks the received data and sends the response message after it received data.

The length of a data communications sequence program can be shortened by using the bidirectional mode.

(3) The communications mode using the RS-232C interface can be set to either full-duplex or half-duplex:

The communications mode using the RS-232C interface of the AJ71C24-S8 can be switched either to full-duplex or half-duplex according to the specifications of the peripheral device.

(4) Multidrop link with more than one computer is possible:

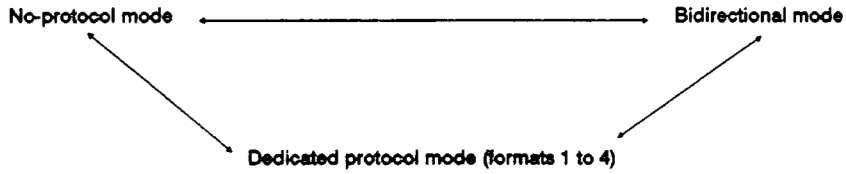
More than one computer can be put into a multidrop link with the AJ71C24-S8.

The PC CPU modules in the multidrop link can be accessed from the computers for read/write of device data and sequence programs.

(5) and (6) are the additional functions when compared with the AJ71C24-S6

(5) Mode switching function when the AJ71C24-S8 operates

The AJ71C24-S8's RS-232C/RS-422 interface can be switched between the following modes after a start-up:



(6) Transmission control function using DC1/DC3 and DC2/DC4

Data communications between the AJ71C24 and an external device can be controlled by using the DC1/DC3 and DC2/DC4 codes.

DC1/DC3 send control, DC1/DC3 receive control: Enables or disables data send and receive.

DC2/DC4 send control, DC2/DC4 receive control: Controls the valid range of send/receive data.

REMARK

If any existing programs are used with the AJ71C24-S8, see Appendix 1.2.3 for interchangeability between the AJ71C24-S8 and the following devices.

- AJ71C24 computer link modules
- AJ71C24-S3 computer link modules
- AJ71C24-S6 computer link modules

1.1 Features

The features of the AJ71C24-S8 computer link module (hereafter called the AJ71C24 in this manual) are given below.

1.1.1 Control operations in data communications

Data transmission operations between an AJ71C24 and external devices (e. g., computers) can be controlled using either the dedicated protocols (*1) or in the no-protocol/bidirectional mode. These control operations can be selected individually with the RS-232C and RS-422 ports of an AJ71C24.

(1) Communications using the dedicated protocols

(a) Communications at the request of the computer

Data communications is always initiated by the computer.

Designated data is transmitted according to the request command transmitted from a computer to an AJ71C24.

It is not necessary to create and change special sequence programs in order to use an AJ71C24.

1) Read and write possible to and from all PC CPU devices

Data can be read from all PC CPU devices. This permits observation and monitoring of all operations, as well as the collection and analysis of data. Data can be written to all PC CPU devices. This permits production control and production directives to be carried out.

2) An AJ71C24 can upload and download programs from a PC CPU.

PC CPU programs (main sequence and subsequence control programs and microcomputer programs), parameter data and comment data are read by the computer and stored. When required they can be written to the PC CPU to change the program.

3) Remote RUN and STOP control of the PC CPU

The PC CPU can be remote-controlled by means of RUN and STOP instructions from the computer.

4) When multiple computers and PC CPU modules are connected to a link with an AJ71C24 module, the input (X) signals of the CPUs in the link can be turned ON/OFF using any computer in the link. This function can immediately stop or simultaneously start all CPUs in the link.

(This function is called the global function of the AJ71C24.)

(b) Communications at the request of the PC CPU

The PC CPU transmits the data send request.

When the emergency data needs to be transmitted from a PC CPU to a computer, the PC CPU transmits a send request to the AJ71C24 to make the computer execute an interrupt processing.

(This is the on-demand function of the AJ71C24. It is available only when one computer is connected to one PC CPU.)

* 1: The dedicated protocols consist of four different protocols. The term "dedicated protocols" used in this manual is the collective term for these protocols.

(2) Communications in the no-protocol/bidirectional modes

Either the no-protocol mode or the bidirectional mode can be set.

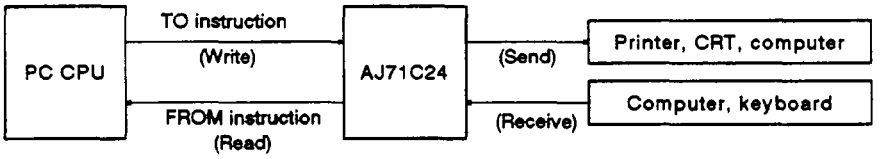
(a) Communications in the no-protocol mode

1) Data communications can be initiated by a PC CPU

Data communications can be initiated by a computer or any PC CPU. Data can be transmitted from a PC CPU to an external device by using the TO instruction in the sequence program to write data to the buffer memory.

Data transmitted from an external device can be read by a PC CPU using the FROM instruction in the sequence program.

The following example shows a system with a printer, CRT and keyboard terminal connected in a 1:1 ratio. Data can be output from the buffer memory to the printer or a CRT display using the TO instruction. Data input from the keyboard to the buffer memory can be read using a FROM instruction from the PC CPU.



2) Receiving data length can be set to variable or fixed:

The Length of the data transmitted from an external device and received by the PC CPU can be set to variable or fixed.

i) Receiving variable-length data:

Data receive stops when the receive completed code set by the user is received.

ii) Receiving fixed-length data:

Data receive stops when the fixed length of data set by the user is received.

Both the receive completed code and the receive-completion data length can be freely set by the user.

3) Variable communications memory area

The user memory area can be allocated to suit the purpose and application of the data transmission.

(b) Bidirectional communications

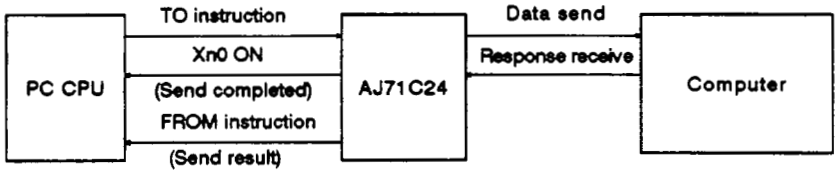
1) Data communications can be initiated by a PC CPU

Data communications can be initiated by a computer or any PC CPU. Data can be transmitted from a PC CPU to an external device by using the TO instruction in the sequence program to write data to the buffer memory.

The data send operation is completed when the response message to the sent (received) data is received from the computer. The result of the send (normal end/error) is stored in the buffer memory and can be read out.

The data received from the computer can be read with the FROM instruction of the sequence program.

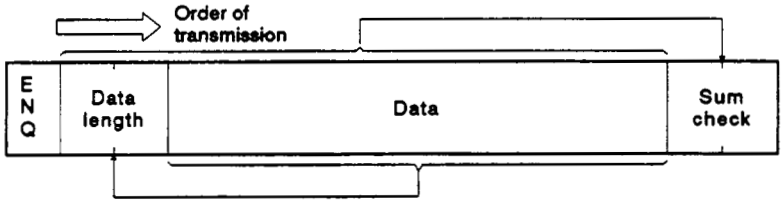
(When data is transmitted by an AJ71C24)



2) Data length is set within the send message

Data length is set within the send message when the data is transmitted to a device.

The receiving side recognizes the data length by the send message.



The send data of the AJ71C24 is processed as follows.

ENQ:..... Added to the head.

Data length:..... The send data length set in the buffermemory is transmitted.

Data:..... The send data stored in the buffer memoryis transmitted.

Sum check:..... Computed with the sum checking range in a message.

The data transmitted by a computer and received by an AJ71C24 is processed as follows.

ENQ:..... Checked and removed from the received data.

Data length:..... Stored in the buffer memory as the received data length.

Data:..... Stored in the buffer memory as the received data.

Sum check:..... Checked and removed from the received data.

3) Variable communications memory area

The user memory area can be allocated to suit the purposes and applications of the data transmission.

1.1.2 System configuration and the number of stations when a computer link system is constructed

A computer link system using the dedicated protocol, no-protocol mode, or bidirectional mode can be constructed by connecting the computer to the PC CPU in the ratios of 1 :1, 1:n, 2:1, 2:n, and m:n. (*1)

When the connection ratio is 1:n or 2:n, up to 32 PC CPU stations can be tied to one link system.

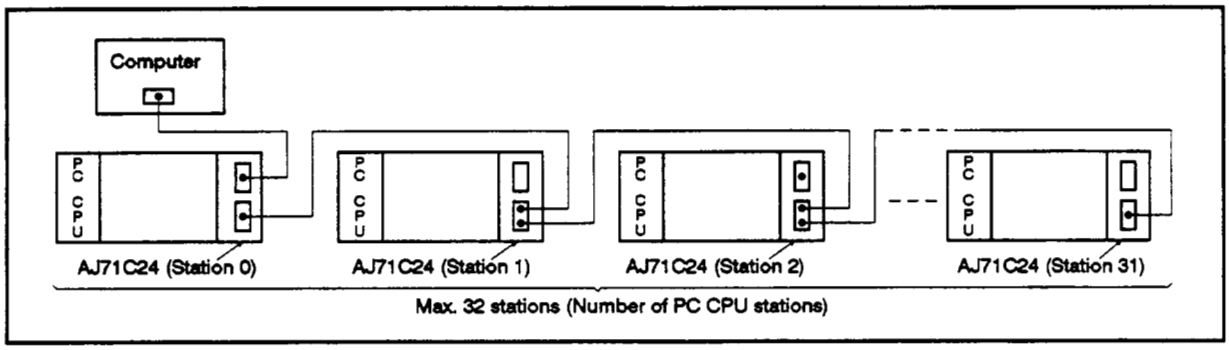
When the connection ratio is m:n, up to 32 stations of computers and PC CPU modules can be tied to one link system.

1) When the connection ratio of the computer to the PC CPU module is 1:n:

   This method of linking uses one computer and multiple PC CPU modules for up to 32 stations.

   Data communications is executed between the computer and designated PC CPU stations.

   This link system is called a multidrop link system.

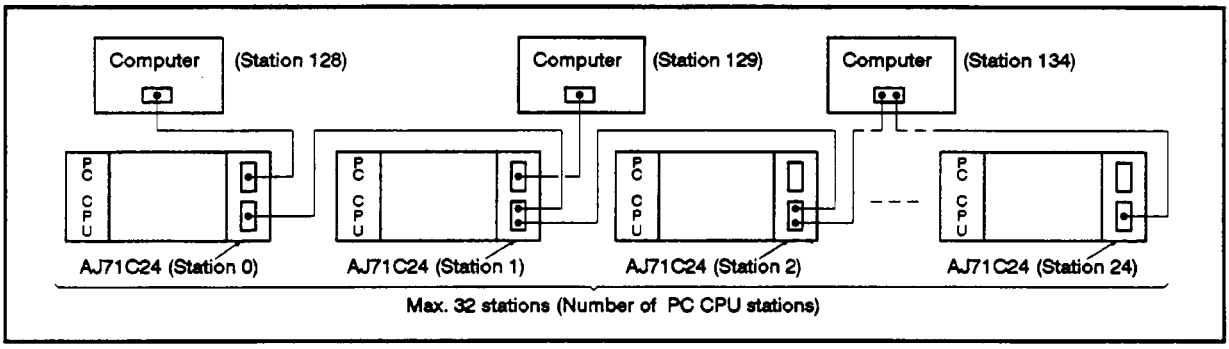


2) When the connection ratio of the computer to the PC CPU module is m:n:

This method of linking uses more than one computers and multiple PC CPU modules for up to 32 stations.

Data communications is executed between a computer (which has acquired the access right through the communications with other computers) and designated PC CPU stations.

This system is also called a multidrop link system.



• 1: The on-demand function and the data communications in the bidirectional mode mentioned respectively in Section 1.1.1 (1)(b) and (2)(b) cannot be used with the multidrop link systems.

1.1.3 Link with a computer through data link systems

In a system connected through the following data link system, if the system contains a PC CPU connected to a computer via an AJ71C24, data communications is possible between the computer and a PC CPU not equipped with the AJ71C24.

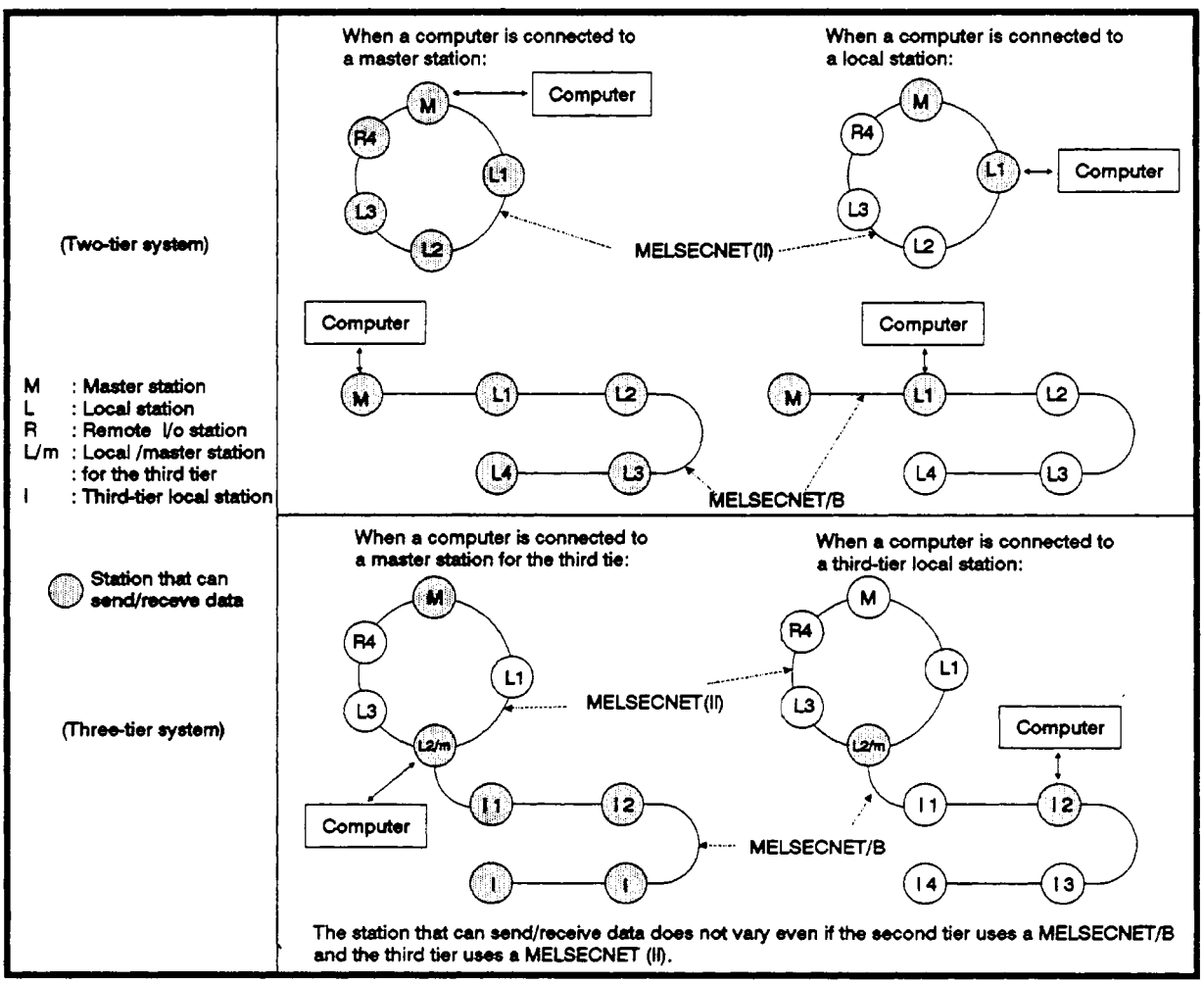
However, communications is not possible with A0J2CPUP23/R23 or A0J2P25/R25 modules.

(1) PC CPU in the MELSECNET (II)

- Master/Local stations:
  Can communicate all data (device memory, programs, etc.).
- Remote I/O station:
  Can communicate only special-function module's buffer data.

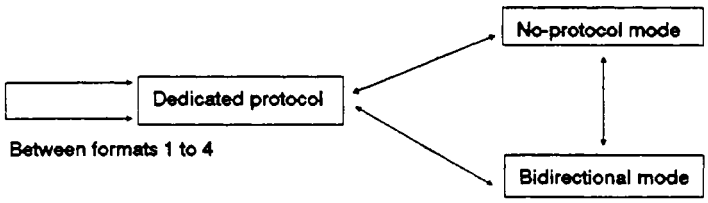
(2) PC CPU in the MELSECNET/B

- Master/Local stations:
  Can communicate all data (device memory, programs, etc.).


(Two-tier system)
M : Master station
L : Local station
R : Remote I/o station
L/m : Local /master station
: for the third tier
I : Third-tier local station
Station that can send/receive data
(Three-tier system)
When a computer is connected to a master station:
When a computer is connected to a local station:
Computer
MELSECNET(II)
MELSECNET/B
When a computer is connected to a master station for the third tie:
When a computer is connected to a third-tier local station:
The station that can send/receive data does not vary even if the second tier uses a MELSECNET/B and the third tier uses a MELSECNET (II).

1.1.4 Mode switching function

After the AJ71C24 has started operating, the AJ71C24's RS-232C/RS-422 interfaces can be switched to another mode.



1.1.5 Transmission control function

Data communications between the AJ71C24 and an external device can be controlled by using DC codes or DTR/DSR signals.

(1) Control using DC1/DC3 or DC2/DC4 codes

- This function can be used for controlling data communications with an external device connected to the AJ71C24 at the RS-232C/RS-422 interface.
- DC1/DC3 control refers to using the DC1 and DC3 codes to notify the communicating device of the enabled/disabled state of data receive.
- DC2/DC4 control refers to using DC2 and DC4 codes to indicate the valid range of send/receive data.
- Data to be sent/received must begin with DC2 code and end with DC4 code.

DC2	Data	DC4

(2) Control using DTR/DSR signals

- This function can be used for data communications with an external device connected to the AJ71C24 at the RS-232C interface.
- DTR/DSR control refers to using the DTR and DSR signals to notify the communicating device of the enabled/disabled state of data receive of the AJ71C24 or external device.
- The AJ71C24 controls the DTR signal as follows:

  When data can be received: Turns ON the DTR signal.

  When data cannot be received: Turns OFF the DTR signal.

- The AJ71C24 controls the DSR signal as follows:

  When the DSR signal is ON: Sends when send data exists.

  When the DSR signal is OFF: Sends only if the DSR is ON when send data exists.

2. SYSTEM CONFIGURATIONS

This section describes system configurations which can be combined with the AJ71C24.

2.1 Overall Configurations

Fig. 2.1 shows the overall configuration of the A series system which is loaded with the AJ71C24.

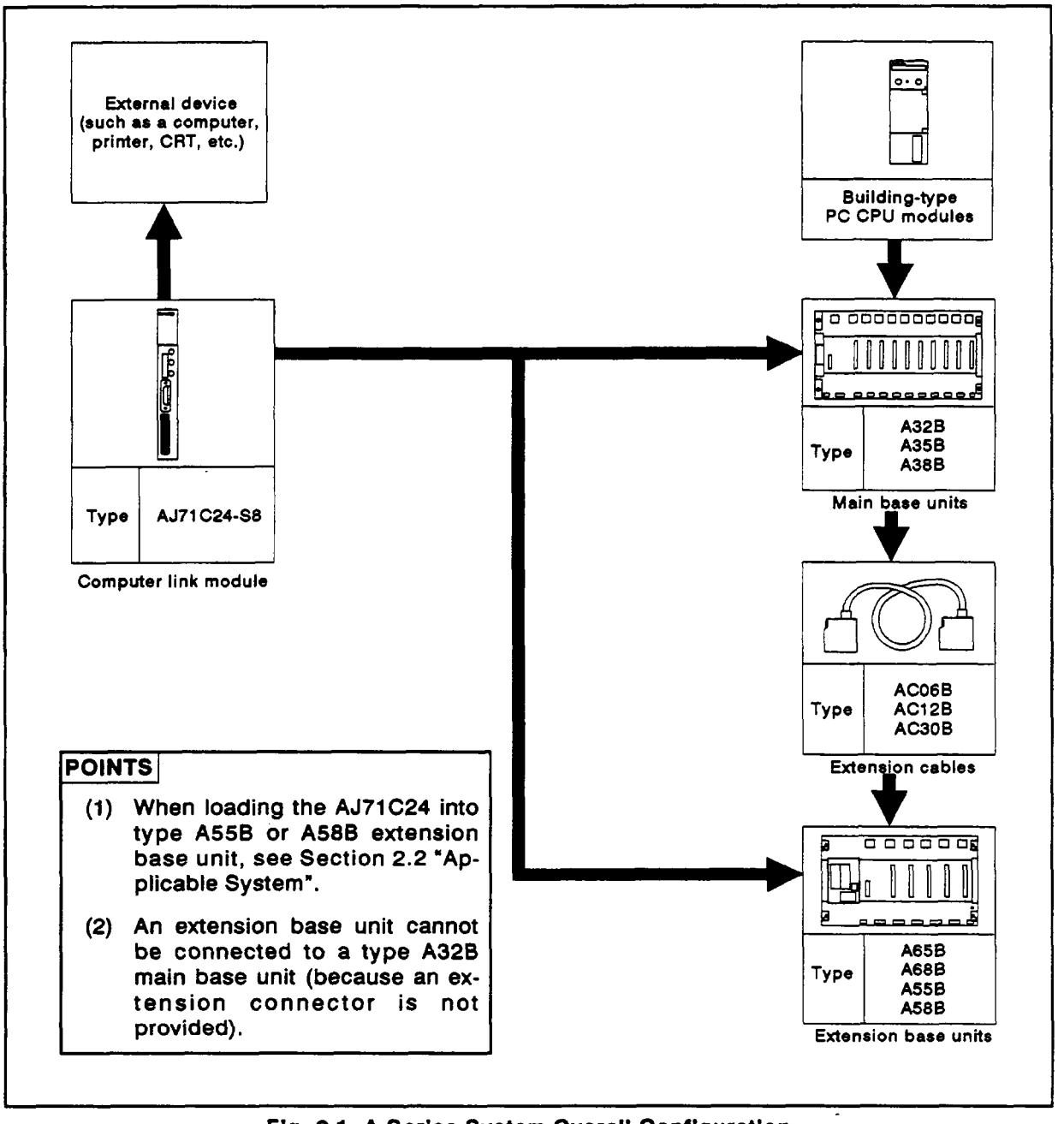


Fig. 2.1 A Series System Overall Configuration

2.2 Applicable Systems

The AJ71C24 can only be used in the systems described below.

(1) Applicable PC CPU modules and the number of AJ71C24 modules

The table below shows the PC CPU modules to which the AJ71C24 is applicable and the number of AJ71C24 modules which can be connected to the PC CPU modules.

The PC CPU modules listed below include those which have the MELSECNET link function.

(e.g., A1CPU includes A1CPUP21/R21 to which an AJ71C24 can be connected.)

PC CPU Modules	Number of Connectable AJ71C24s	Notes
A0J2H A1, A1N A1S A2(-S1), A2N(-S1) A3, A3N A3H, A3M A73	2	If the following modules are used with the AJ71C24, the maximum number of connectable AJ71C24 modules cannot exceed 2 or 6. (See previous column). • AD51(S3)/AD51H Intelligent Communication Module • AD57G Graphic controller Module • AJ71C21(S1) Terminal Interface Module • AJ71C22(S1) Multidrop Link System Module • AJ71C23 Higher Controller High Speed Link Module • AJ71C24(S3/S6) Computer Link Module • AJ71E71 Ethernet Interface Module
A2A(-S1) A3A	6	

(A0J2CPU and A2CCPU are not applicable.)

(2) Applicable base unit

The AJ71C24 can be inserted into any slot of a main base unit or extension base unit with these two exceptions:

(a) The power supply capacity may be insufficient to load the AJ71C24 into an extension base unit with no built-in power supply (A55B or A58B). Wherever possible, avoid loading an AJ71C24 module into this type of extension base unit. If it is necessary to use an AJ71C24 module in an extension base unit with no built-in power supply, it is important to consider (a) the power supply capacity of the main base unit, and (b) the voltage drop along the extension cables when selecting the extension cables.

(b) (The User's Manual of the respective CPU module employed gives details.)

(c) The AJ71C24 should not be loaded into the last slot of the A3CPU extension level 7.

POINTS

(1) The AJ71C24 can also be loaded into the A81CPU base unit (A78B). The A81CPU User's Manual gives the commands available when the AJ71C24 is loaded.

(2) The AJ71C24 cannot be used in a remoto I/O station.

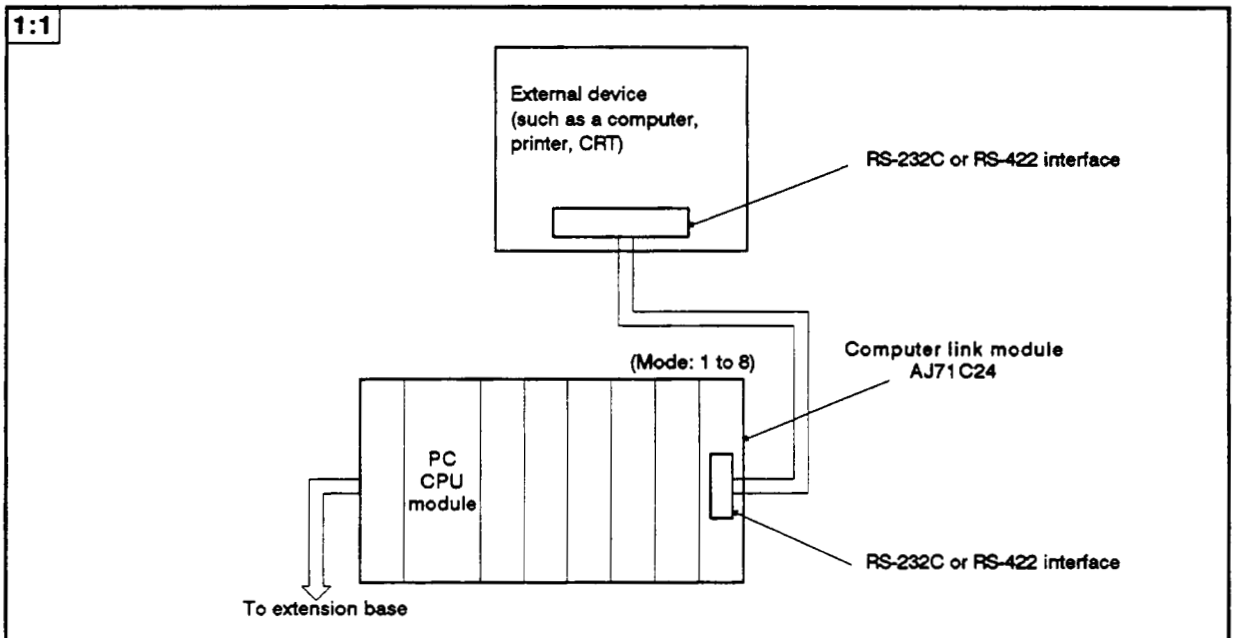
2.3 System Configurations and Available Functions

The AJ71C24 is a link module to connect an external device (such as a computer) and a PC CPU. The system can consist of a single external device and from 1 to 32 PC CPU stations (1 : 1 to 32 ratio system) or two external devices and from 1 to 32 PC CPU stations (2 : 1 to 32 ratio system). The connection may be made in two ways: using the RS-232C port or the RS-422 port.

2.3.1 1 : 1 ratio of an external device (computer) to a PC CPU

(1) The system configuration for a 1 : 1 ratio of an external device (such as a computer) to a PC CPU is shown in Fig. 2.2 below.

(Mode: [ ] - [ ]) in the figure indicates the range of setting set with the mode setting switch of an AJ71C24 (see Section 4.3.1).



POINTS

(1) Use of the RS-232C and the RS-422 interfaces differs in that the RS-422 is used to connect long distances (up to 500 m (1640.5 ft)) and the RS-232C is used to connect short distances (a maximum of 15 m (49.2 ft)).

(2) To have the RS-232C communicate over a distance greater than 15 m (49.2 ft), use a modem or RS-232C/RS-422 converter between the external device and the AJ71C24.

Fig. 2.2 System Configurations (I)

(2) The following tables list the functions available when an external device is linked with a PC CPU module to make a 1 : 1 configuration.

(a) The interface used to set dedicated protocols 1 to 4:

1) Functions available when using an external device

Available Functions		Interfaces for Dedicated Protocol		Note
		RS-422	RS-232C	
Device memory	Read/write	o	o	Including extension devices
	Test			
	Monitor			
Extension file registe	Read/write	o	o	-
	Test			
	Monitor			
Buffer memory AJ71C24 of the self	Read/write	o	o	
Special function module's buffer memory	Read/write	o	o	
Sequence/ Microcomputer program	Read/write	o	o	
Comment	Read/write	o	o	Including extension comments
Parameter	Read/write	o	o	-
PC CPU	Remote RUN/STOP	o	o	
	PC CPU type read	o	o	
Global	Input signal (X) ON/OFF	o	o	
Self-loopback test	Transmission of received data	o	o	

2) Functions available when using a PC CPU

Available Functions		Interfaces for Dedicated Protocol		Note
		RS-422	RS-232C	
On-demand	Data transmission to external devices	o	o	-

(b) Interfaces used to set the no-protocol mode

Functions available when using an external device and a PC CPU

Available Functions		Interfaces for No-protocol Mode		Note
		RS-422	RS-232C	
Send	PC CPU to external device	o	o	To computers, printers, and CRTs.
Receive	External device to PC CPU	o	o	From computers and keyboards

(c) Interfaces used to set the bidirectional mode

Functions available when using an external device and a PC CPU

Available Functions		Interfaces for Bidirectional Mode		Note
		RS-422	RS-232C	
Send	PC CPU to computer	o	o	To computers
Receive	Computer to PC CPU	o	o	From computers

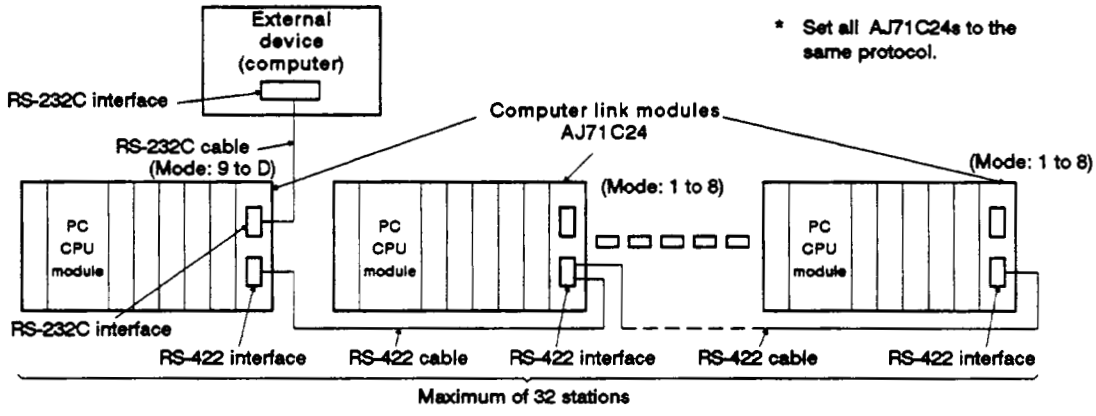
2.3.2 1 : n ratio of an external device to PC CPUs

(1) The system configurations for a 1 : n (up to 32 stations) ratio of an external device (such as a computer) to PC CPUs are shown in Fig. 2.3 below.

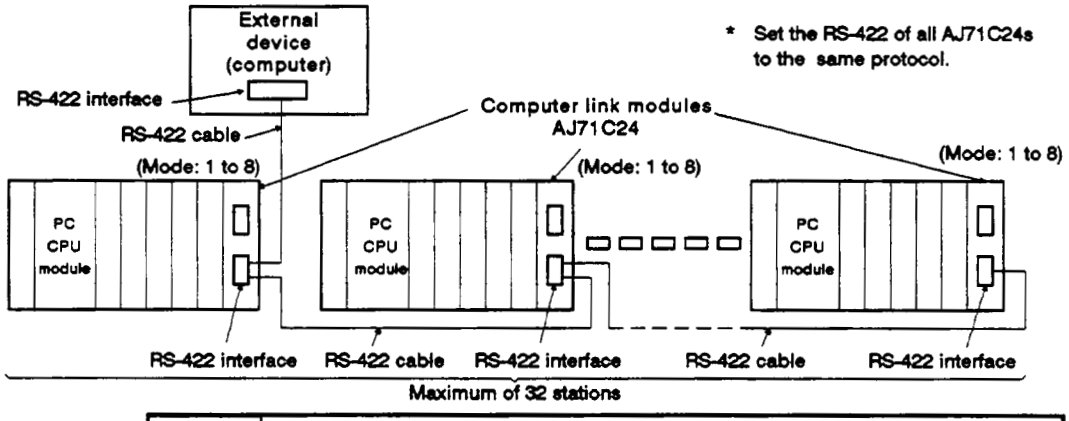
(Mode: [ ] to [ ]) in the figure the range of setting set with the mode setting switch of an AJ71C24 (see Section 4.3.1).

1:n

System configuration 1 The external device is connected to the AJ71C24 modules using the RS-232C



System configuration 2 The external device is connected to the AJ71C24 modules using the RS-422



POINTS

(1) When the mode setting is 5 to 8, the RS-232C interface which is not used for the multidrop link can be used for communications with a computer, a printer, or a CRT in a no-protocol/bidirectional mode.

(2) Use of the RS-232C and the RS-422 interfaces differs in that the RS-422 is used to connect long distances (up to 500 m (1640.5 ft)) and the RS-232C is used to connect short distances (up to maximum of 15 m (49.2 ft)).

(3) To have the RS-232C communicate over a distance greater than 15 m (49.2 ft), use a modem or RS-232C/RS-422 converter between the external device and the AJ71C24.

Fig. 2.3 System Configurations (II)

(2) The following tables list the functions available when an external device is linked with the PC CPU modules to make a 1 : n configuration.

(a) The interface used to set dedicated protocols 1 to 4:

1) Functions available when using an external device

Available Functions		Interfaces for Dedicated Protocol		Note
		RS-422	RS-232C	
Device memory	Read/write	o	o	Including extension devices
	Test			
	Monitor			
Extension file register	Read/write	o	o	-
	Test			
	Monitor			
Buffer memory AJ71C24 of the self	Read/write	o	o	
Special function module's buffer memory	Read/write	o	o	
Sequence/ microcomputer program	Read/write	o	o	
Comment	Read/write	o	o	Including extension comments
Parameter	Read/write	o	o	-
PC CPU	Remote RUN/STOP	o	o	
	PC CPU type read	o	o	
Global	Input signal (X) ON/OFF	o	o	
Self-loopback test	Transmission of received data	o	o	

2) Functions available when using a PC CPU

Available Functions		Interfaces for Dedicated Protocol		Note
		RS-422	RS-232C	
On-demand	Data transmission to external devices	x	x	-

(b) Interfaces used to set the no-protocol mode

Functions available when using an external device and a PC CPU

Available Functions		Interfaces for No-protocol Mode		Note
		RS-422	RS-232C	
Send	PC CPU to external device	o	o*1	To computers, printers, and CRTs.
Receive	External device to PC CPU	o	o*1	From computers and keyboards

*1 : If the external device is capable of performing full-duplex transmission, data communications in the no-protocol mode can be performed.

(c) Interfaces used to set the bidirectional mode

Functions available when using an external device and a PC CPU.

Available Functions		Interfaces for Bidirectional Mode		Note
		RS-422	RS-232C	
Send	PC CPU to computer	x	x	To computers
Receive	Computer to PC CPU	x	x	From computers

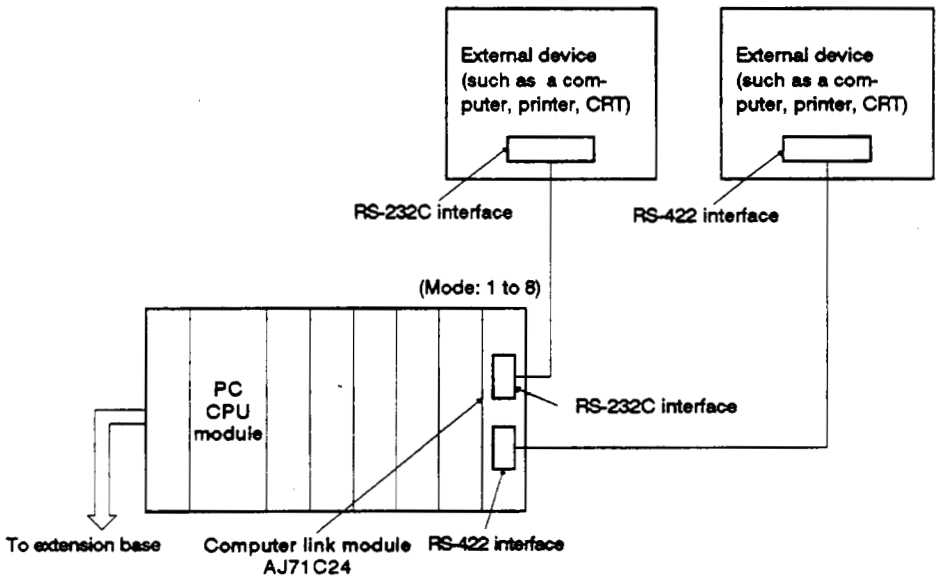
2.3.3 2 : 1 ratio of external devices to a PC CPU

(1) The system configuration for a 2 : 1 ratio of external devices (such as a computer) to a PC CPU is shown in Fig. 2.4 below.

(Mode: [ ] to [ ]) in the figure indicates the range of setting designated with the mode setting switch of an AJ71C24 (see Section 4.3.1).

2:1

(A combination of two systems each of which has a 1 : 1 configuration.)



POINTS

(1) One of the two interfaces is set to a dedicated protocol 1, 2, 3, or 4. The other is set to a no-protocol/bidirectional mode.

(2) The use of the RS-232C and the RS-422 interfaces differs in that the RS-422 is used to connect long distances (up to 500 m (1640.5 ft)) and the RS-232C is used to connect short distances (maximum of 15 m (49.2 ft)).

(3) To have the RS-232C communicate over a distance greater than 15 m (49.2 ft), use a modem or RS-232C/RS-422 converter between the external device and the AJ71C24.

Fig. 2.4 System Configurations (III)

(2) The following tables list the functions available when the external devices are linked with the PC CPU modules to make a 2 : 1 configuration.

(a) The interface used to set dedicated protocols 1 to 4:

1) Functions available when using external devices

Available Functions		Interfaces for Dedicated Protocol		Note
		RS-422	RS-232C	
Device memory	Read/write	o	o	Including extension devices
	Test			
	Monitor			
Extension file register	Read/write	o	o	-
	Test			
	Monitor			
Buffer memory AJ71C24 of the self	Read/write	o	o	
Special function module's buffer memory	Read/write	o	o	
Sequence microcomputer program	Read/write	o	o	
Comment	Read/write	o	o	Including extension comments
Parameter	Read/write	o	o	-
PC CPU	Remote RUN/STOP	o	o	
	PC CPU type read	o	o	
Global	Input signal (X) ON/OFF	o	o	
Self-loopback test	Transmission of received data	o	o	

2) Functions available when using a PC CPU

Available Functions		Interfaces for Dedicated Protocol		Note
		RS-422	RS-232C	
On-demand	Data transmission to external devices	o	o	-

(b) Interfaces used to set the no-protocol mode

Functions available when using external devices and a PC CPU

Available Functions		Interfaces for No-protocol Mode		Note
		RS-422	RS-232C	
Send	PC CPU to external device	o	o	To computers, printers, and CRTs.
Receive	External device to PC CPU	o	o	From computers and keyboards

(c) Interfaces used to set the bidirectional mode

Functions available when using external devices and a PC CPU

Available Functions		Interfaces for Bidirectional Mode		Note
		RS-422	RS-232C	
Send	PC CPU to computer	o	o	To computers
Receive	Computer to PC CPU	o	o	From computers

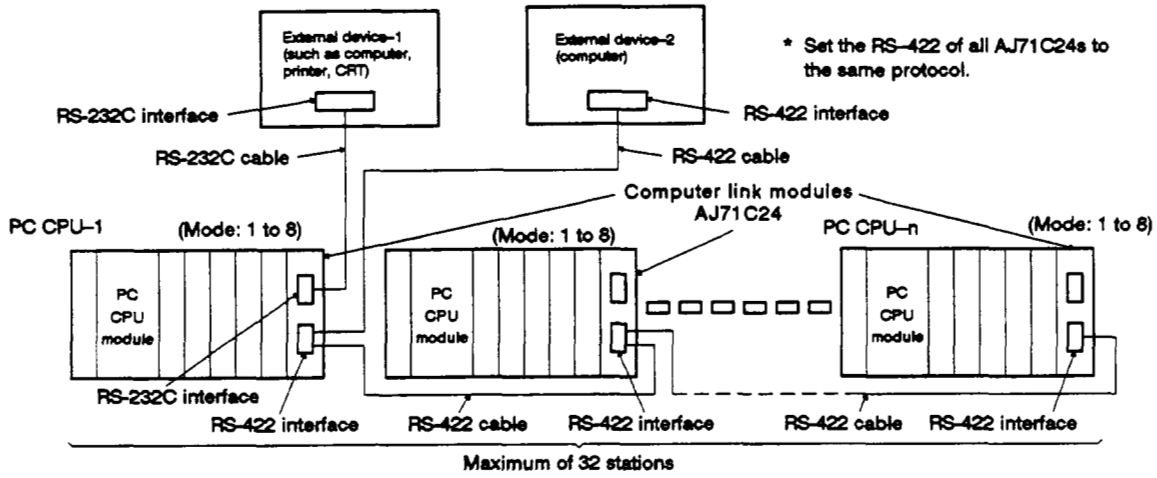
2.3.4 2 : n ratio of external devices to PC CPUs

(1) The system configuration for a 2 : n (up to 32 stations) ratio of external devices (such as a computer) to PC CPUs is shown in Fig. 2.5 below.

(Mode: [ ] to [ ]) in the figure indicates the range of setting set with the mode setting switch of an AJ71C24 (see Section 4.3.1).

2:n

(A combination of two systems one of which has a 1 : 1 configuration and the other has a 1 : n configuration.)



POINTS

(1) One of the two interfaces of the AJ71C24 which is connected to the external devices is set to a dedicated protocols 1, 2, 3, or 4. The other is set to a no-protocol/bidirectional mode.

(2) When the mode setting is 5 to 8, the RS-232C interface which is not used for the multidrop link can be used for communications with a computer, a printer, or a CRT in a no-protocol/bidirectional mode.

(3) To have the RS-232C communicate over a distance greater than 15 m (49.2 ft), use a modem or RS-232C/RS-422 converter between the external device and the AJ71C24.

Fig. 2.5 System Configurations (IV)

(2) The following tables list the functions available when the external devices are linked with the PC CPU modules making a 2 : n configuration.

(a) The interface used to set dedicated protocols 1 to 4:

1) Functions available when using external devices

Available Functions		Interfaces for Dedicated Protocol		Note
		RS-422	RS-232C	
Device memory	Read/write	o	o	Including extension devices
	Test	o	o	
	Monitor	o	o	
Extension file register	Read/write	o	o	-
	Test	o	o	
	Monitor	o	o	
Buffer memory AJ71C24 of the self	Read/write	o	o	
Special function module's buffer memory	Read/write	o	o	
Sequence/ microcomputer program	Read/write	o	o	
Comment	Read/write	o	o	Including extension comments
Parameter	Read/write	o	o	-
PC CPU	Remote RUN/STOP	o	o	
	PC CPU type read	o	o	
Global	Input signal (X) ON/OFF	o	o	
Self-loopback test	Transmission of received data	o	o	

2) Functions available when using PC CPUs

Available Functions		Interfaces for Dedicated Protocol		Note
		RS-422	RS-232C	
On-demand	Data transmission to external devices	o*1	o*1	-

* 1 : Data communications is possible only with the system which has a 1 : 1 configuration (one external device to one PC CPU, as shown in Fig. 2.5).

(b) Interfaces used to set the no-protocol mode

Functions available when using external devices and PC CPUs

Available Functions		Interfaces for No-protocol Mode		Note
		RS-422	RS-232C	
Send	PC CPU to external devices	o	o*1	To computers, printers, and CRTs.
Receive	External device to PC CPU	o	o*1	From computers and keyboards

* 1 : If full-duplex transmission is possible with the external device, data communications in the no-protocol mode is possible with the system which has the 1 : n configuration (external device-2 to PC CPUs, as shown in Fig. 2.5).

(c) Interface used to set the bidirectional mode

Functions available when using external devices and PC CPUs

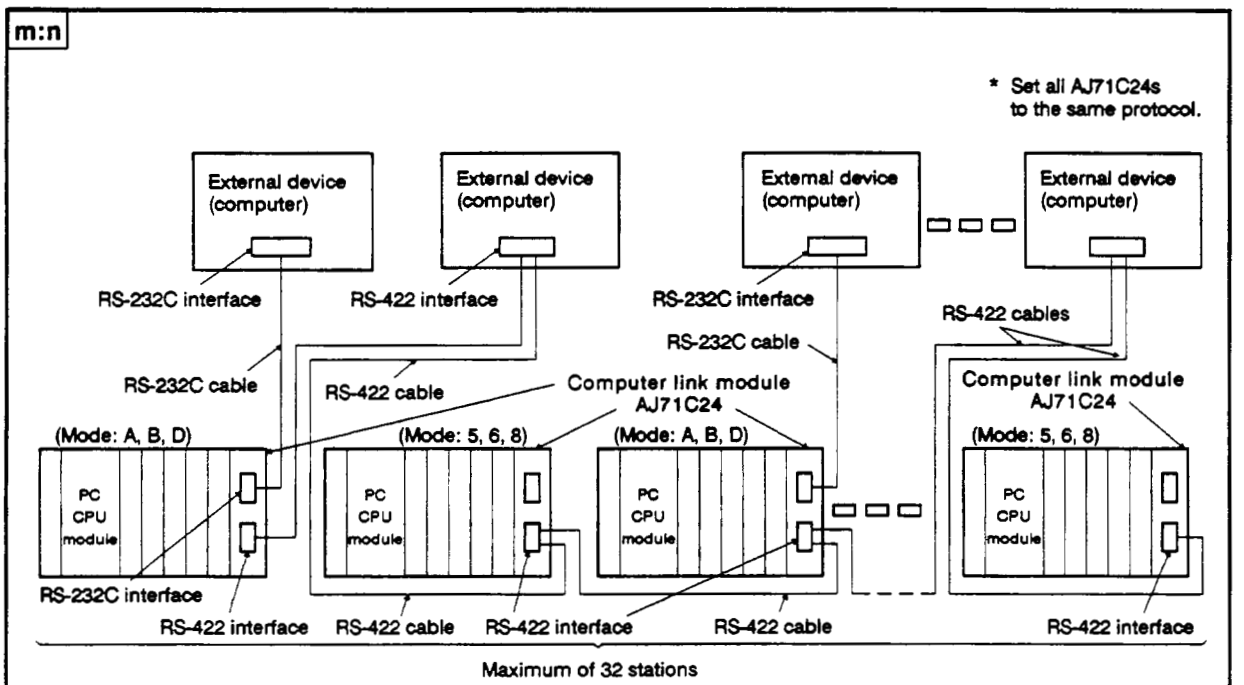
Available Functions		Interfaces for Bidirectional Mode		Note
		RS-422	RS-232C	
Send	PC CPU to computer	o*1	o*1	To computers
Receive	Computer to PC CPU	o*1	o*1	From computers

* 1 : Data communications is possible only with the system which has a 1 : 1 configuration (external device-1 to one PC CPU, as shown in Fig. 2.5).

2.3.5 m : n ratio of external devices to PC CPUs

(1) The system configuration for a m : n (up to 32 stations) ratio of external devices (such as a computer) to PC CPUs is shown in Fig. 2.6 below.

(Mode: [ ], [ ], [ ]) in the figure indicates setting set with the mode setting switch of an AJ71C24 (see Section 4.3.1).



POINTS

(1) All the external devices and AJ71C24 modules are connected to form a multidrop link in the above example which uses dedicated protocols 1, 2, or 4. The multidrop link of the m : n ratio system configuration cannot use dedicated protocol 3.
When multiple external devices and AJ71C24 modules are used to form a multidrop link, the procedure to exercise the access right with a specific station should be provided.

(2) When the mode setting is 5 to 8, the RS-232C interface which is not used for the multidrop link can be used for communications with a computer, a printer, or a CRT in a no-protocol/bidirectional mode.

(3) To have the RS-232C communicate over a distance greater than 15 m (49.2 ft), use a modem or RS-232C/RS-422 converter between the external device and the AJ71C24.

Fig. 2.6 System Configurations (V)

(2) The following tables list the functions available when the external devices are linked with the PC CPU modules making an m : n configuration.

(a) The interface used to set dedicated protocols 1, 2, 4:

1) Functions available when using external devices

Available Functions		Interfaces for Dedicated Protocol		Note
		RS-422	RS-232C	
Device memory	Read/write	o	o	Including extension devices
	Test	o	o	
	Monitor	o	o	
Extension file register	Read/write	o	o	-
	Test	o	o	
	Monitor	o	o	
Buffer memory AJ71C24 of the self	Read/write	o	o	
Special function module's buffer memory	Read/write	o	o	
Sequence/ microcomputer program	Read/write	o	o	
Comment	Read/write	o	o	Including extension comments

* If full-duplex transmission is possible with the external device, data communications in the dedicated protocol mode is possible with the RS-232C interface.

2) Functions available when using a PC CPU

Available Functions	Interfaces for Dedicated Protocol		Note
	RS-422	RS-232C	

(b) Interfaces used to set the no-protocol mode (Mode: for stations set to 5, 6, or 8)

Functions available when using external devices and the PC CPU

Available Functions		Interfaces for No-protocol Mode		Note
		RS-422	RS-232C	
Send	PC CPU to external devices	-	o	To computers, printers, and CRTs.

(c) Interfaces used to set the bidirectional mode (Mode: for stations set to 5, 6, or 8)

Functions available when using external devices and the PC CPU

Available Functions		Interfaces for Bidirectional Mode		Note
		RS-422	RS-232C	
Send	PC CPU to computer	-	o*1	To computers

*1 : Data communications is possible only with the 1 : 1 ratio configuration.

2.3.6 Links with an external device (such as a computer) through data link systems

By installing the AJ71C24 to a PC CPU linked with other PC CPUs on data link systems, communications is possible with other PC CPU stations on MELSECNET(II), MELSECNET/B.

However, communications is not possible with A0J2CPUP23/R23 or A0J2CPUP25/R25 modules.

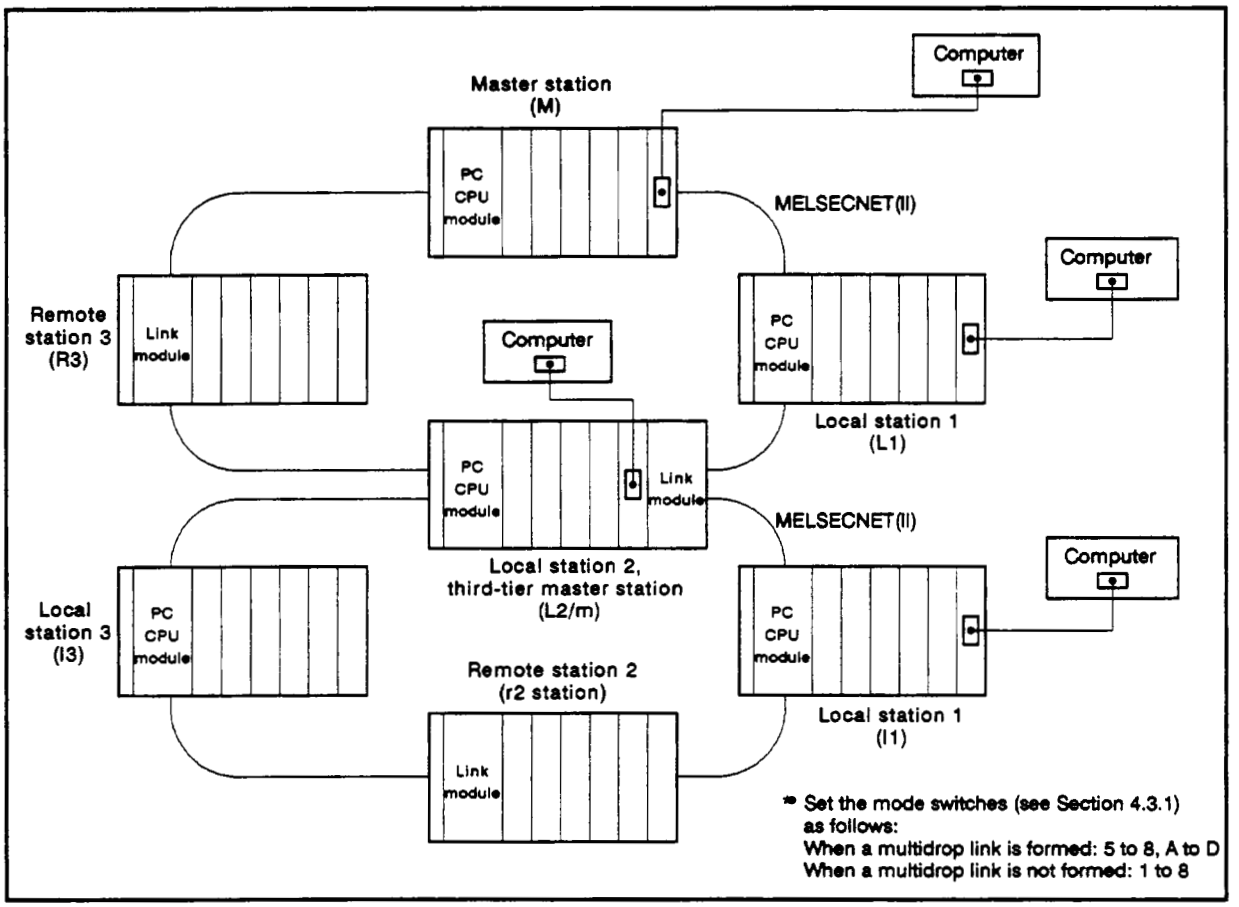


Fig. 2.7 System Configurations (VI)

Range of PC CPUs with which communications is possible:

(PC CPUs equipped with AJ71C24)	(MELSECNET (II), MELSECNET/B stations with which communications is possible)
• M station (master station)	(1) The self
	(2) All second-tier local stations (L1, L2/m)
	(3) Second-tier remote I/O stations equipped with a special function module (R3)
• L stations (local stations)	(1) The self
	(2) Second-tier master station (M station)
• L/m station (local/third-tier master station)	(1) The self
	(2) Second-tier master station (M station)
	(3) All third-tier local stations (I1, I3)
	(4) Third-tier remote I/O stations equipped with a special function module (r2)
• I station (third-tier local stations)	(1) The self
	(2) Third-tier master station (M station) (L2/m)

MEMO

3. SPECIFICATIONS

3.1 General Specifications

Table 3.1 General Specifications

Item	Specifications				
Operating ambient temperature	0 to 55°C (32 to 131°F)				
Storage ambient temperature	–20 to 75° (4 to 167°F)				
Operating ambient humidity	10 to 90% RH, no condensation				
Storage ambient humidity	10 to 90% RH, no condensation				
Vibration resistance	Conforms to **JIS C 0911	Frequency	Acceleration	Amplitude	Sweep Count
		10 to 55 Hz	—	0.075 mm (0.003 inch)	10 times *(1 octave/ minute)
		55 to 150 Hz	9.8 m/s^2 (1 g)	—	
Shock resistance	Conforms to JIS C 0912 (98 m/s^2 (10g) x 3 times in 3 directions)				
Noise resistance	By noise simulator 1500 V.P.P. noise voltage, 1 μsec noise width and 25 to 60 Hz noise frequency				
Dielectric withstand voltage	500 VAC for 1 minute across batch of DC external terminals and ground				
Insulation resistance	50 MΩ or more with 500 VDC insulation resistance tester at the same location as dielectric strength.				
Operating ambience	No corrosive gases or dust.				
Cooling method	Self-cooling				

REMARK

(1) One octave marked * indicates a change from the initial frequency to double or half frequency. For example, any of the changes from 10 Hz to 20 Hz, 20 Hz to 40 Hz, 40 Hz to 20 Hz, and 20 Hz to 10 Hz are referred to as one octave.

(2) The noise durability and dielectric withstand voltage values were obtained with the RS-232C and RS-422 interfaces unconnected.

** JIS: Japanese Industrial Standard

3.2 Performance Specifications

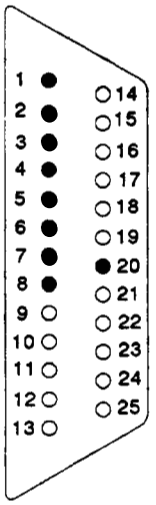
3.2.1 Transmission specifications

Table 3.2 Transmission Specifications

Item		Specifications		
Interface		Conform to RS-232C.		
		Conform to RS-422.		
Transmission method		RS-232C	Dedicated protocol	Half-duplex communications system *1
			No-protocol/bidirectional	Full-/half-duplex (buffer memory setting)
		RS-422	Dedicated protocol	Half-duplex communications system *1
			No-protocol/bidirectional	Full-duplex communications system
Synchronous system		Asynchronous system		
Transmission system		300, 600, 1200, 2400, 4800, 9600, 19200 BPS (switch selected)		
Data format	Start bit	1		
	Data bit	7 or 8		Selectable
	Parity bit	1 or none *4		
	Stop bit	1 or 2		
Access cycle		Each request is processed in the END processing of the sequence program. Therefore, access cycle is 1 scan time.		
Error detection		Parity check present (odd/even)/absent		
		Sum check present/absent		
DTR/DSR (ER/DR) control		Present /Absent (RS-232C only)		
DC1/DC3, DC2/DC4 control		Present /Absent		
System configuration (External device: PC CPU)		Dedicated protocol		1 : 1, 1 : n, m : n *2
		No-protocol		1 : 1, 1 : n *2
		Bidirectional		1 : 1
Transmission distance		Up to 15 m (49.2 ft) for RS-232C		
		Up to 500 m (1640.5 ft) for RS-422		
Current consumption		5 VDC, 1.4 A		
Number of occupying I/Os		32 *3		
Weight		630 g (1.39 lb)		
Recommended cable (for RS-422)		RS-422 SPEV(SB)- MPC - 0.2 x 3P		
Recommended RS-232C to RS-422 converter		EL-LINE-M		

*1: If the on-demand function is used, only full-duplex communications is available when full-duplex communications is enabled.
*2: "n" for 1:n ratio is up to 32. Total of "m" and "n" for m:n ratio is up to 32.
*3: Set the special function modules to have 32 inputs/outputs when the I/O allocation is set.
*4: Horizontal parity

3.2.2 RS-232C connector specifications



Pin Number	Name	Signal Abbreviation	Signal Direction AJ71C24 ↔ Computer
1	Frame ground	FG	⟷
2	Send data	SD (TXD)	→
3	Receive data	RD (RXD)	←
4	Request to send	RS (RTS)	→
5	Clear to send	CS (CTS)	←
6	Data set ready	DSR (DR)	←
7	Signal ground	SG	⟷
8	Receive carrier detection	CD	←
20	Data terminal ready	DTR (ER)	→

Fig. 3.1 RS-232C Connector Specifications

(1) Signals are described below.

(a) FG signal

Connect the cable shield to pin 1 of the AJ71C24. If both the computer and the AJ71C24 have an FG pin, connect the cable shield to one of the FG pins only.

If the cable shield is connected to both FG pins, the resulting noise may prevent correct data communications.

(b) RS signal

The AJ71C24 system turns ON/OFF the RS signal according to the setting of the CD terminal check (see Section 7.1) and the transmission method (see Section 7.2), as shown below.

Transmission Method	CD terminal Check Setting	State of the CD Signal	RS Signal ON/OFF Control
Full-duplex	Enabled	ON	When the AJ71C24 is in the ready state, the AJ71C24 system turns RS signal ON.
		OFF	The AJ71C24 system turns the RS signal OFF.
	Disabled	ON	When the AJ71C24 is in the ready state, the AJ71C24 system turns the RS signal ON. (normally ON)
		OFF	
Half-duplex	Enabled (always set to enabled)	ON	See Section 5.
		OFF	

Data transmission from the external device should be done confirming the RS signal controlled by the AJ71C24.

(c) CS signal

Data is only transmitted from the AJ71C24 when this signal is ON.

(d) DSR signal

- During DTR/DSR control, when this signal is OFF, data is not transmitted from the AJ71C24 to an external device.
- If DTR/DSR control is not executed, the DSR signal status will be ignored.
- When the external device can receive data, make sure that this signal is ON.

(e) CD signal

The AJ71C24 operates according to the setting of the CD terminal check.

	CD Terminal Check Enabled	CD Terminal Check Disabled
Full-duplex	The AJ71C24 performs transmission processing when the CD signal (receive carrier detection) is ON. The transmission sequence of the AJ71C24 is initialized when the CD signal is turned OFF during data communications in the dedicated protocol.	The AJ71C24 performs transmission processing regardless of the ON/OFF state of the CD signal. (This enables data communications with those external devices which cannot control (ON/OFF) the CD signal.)
Half-duplex	See Section 5.	Setting impossible

(f) DTR signal

The AJ71C24 system controls the DTR signal as follows:

The AJ71C24 system turns ON the DTR signal when communications is enabled if the dedicated protocol or bidirectional mode is currently used.

When DTR/DSR control is executed, the AJ71C24 system turns ON/OFF the DTR signal according to the size of available area of the receive data storage OS area during communications in the no-protocol mode. (The DTR signal turns ON when the data communications of the AJ71C24 is enabled.)

Section 3.5.2 gives for the ON/OFF timing of the DTR signal.

Since the received data is stored in the OS area when the DTR signal is OFF, read the received data using the sequence program (See Section 9).

This signal is ON during DTR/DSR control.

(2) ON/OFF definitions are as follows:

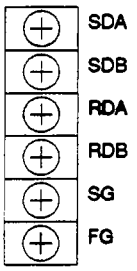
ON : 5V to 15 VDC
OFF : −5 V to −15 VDC

(3) Interface connector

The following type of RS-232C connector is used. Use a matching connector.

25-pin D-sub (female) screw-fixing type

3.2.3 RS-422 terminal block specifications



Signal Abbreviation	Signal Direction AJ71C24 ↔ Computer	Description
SDA	→	Send data
SDB	→	Send data
RDA	←	Receive data
RDB	←	Receive data
SG	↔	Signal ground
FG	↔	Frame ground

Fig. 3.2 RS-422 Terminal Block Specifications

(1) Fig. 3.3 shows the RS-422 function block diagram.

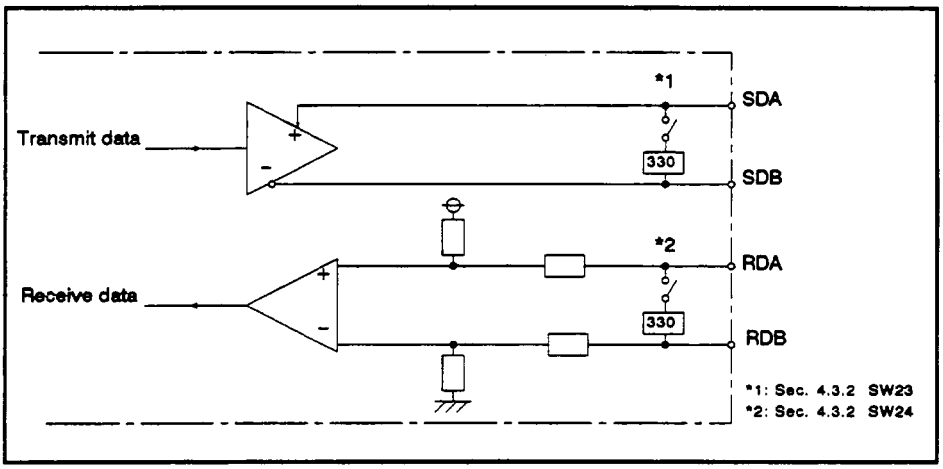


Fig. 3.3 RS-422 Function Block Diagram

3.2.4 RS-422 cable specifications

An RS-422 cable is recommended in Section 3.2.1. Other types of cables may be used instead, if they conform to the specifications listed in the following table.

Item	Description
Cable type	Shielded cable
Number of pairs	3 Pairs
Conductor resistance (20°C)	88.0 Ω/km or less
Insulation resistance	10.000 MΩ km or less
Dielectric strength	500 VDC, 1 minute
Electrostatic capacity (1 KHz)	60 nF/km or less on average
Characteristic impedance (100 KHz)	110 ± 10 Ω

Fig. 3.4 RS-422 Cable Specifications (km = 0.621 mile)

3.3 Data Communications Functions

The tables below list the data communications functions available when an external device (such as a computer) and a PC CPU are connected by an AJ71C24 module.

3.3.1 Functions available using dedicated protocols and commands

The functions available using dedicated protocols 1 to 4 are listed in Tables 3.3 and 3.4.

The commands in Table 3.3 are the ACPU common commands that are employed when a CPU module (see Section 2.2) is used together with an AJ71C24.

The commands in Table 3.4 are the AnACPU dedicated commands that are employed when the A2ACPU(P21/R21)(-S1) or A3ACPU(P21/R21) is used together with an AJ71C24.

Use the commands in Table 3.4 to access the AnACPU device memory. Read/write of data can be done with the whole area of each device memory.

The functions in Tables 3.3 and 3.4 are also available when a multidrop link of 1:n or m:n ratio configuration is made and when a computer link is made using the data link system.

(1) Functions available with the ACPU common commands

Table 3.3 Functions List When Using a Dedicated Protocol

Function			Command: Symbol	Command: ASCII Code	Description	Number of Point Processed per Communications
Device memory	Batch read	Bit units	BR	42H, 52H	Reads bit devices (such as X, Y, M) in units of 1 device.	256 points
		Word units	WR	57H, 52H	Reads bit devices (such as X, Y, M) in units of 16 devices.	32 words (512 points)
					Reads word devices (such as D, R, T, C) in units of 1 device.	64 points
	Batch write	Bit units	BW	42H, 57H	Writes bit devices (such as X, Y, M) in units of 1 device.	160 points
		Word units	WW	57H, 57H	Writes bit devices (such as X, Y, M) in units of 16 devices.	10 words (160 points)
					Writes word devices (such as D, R, T, C) in units of 1 device.	64 points
	Test (random write)	Bit units	BT	42H, 54H	Specifies bit devices (such as X, Y, M) and device number in units of 1 device at random and sets/resets the device.	20 points
		Word units	WT	57H, 54H	Specifies bit devices (such as X, Y, M) and device number in units of 16 devices at random and sets/resets the device.	10 words (160 points)
					Specifies word devices (such as D, R, T, C) and device number in units of 1device at random and sets/resets the device.	10 points
	Monitor data entry	Bit units	BM	42H, 4DH	Sets bit devices to be monitored (such as X, Y, M) in units of 1 device.	40 points *1
		Word units	WM	57H, 4DH	Sets bit devices to be monitored (such as X, Y, M) in units of 16 devices.	20 words *1 (320 points)
					Sets word devices to be monitored (such as D, R, T, C) in units of 1 device.	20 points
	Monitor	Bit units	MB	4DH, 42H	Reads data from devices for which device data registration has been made.	—
		Word units	MN	4DH, 4EH		
Extension file register	Batch read		ER	45H, 52H	Reads extension file registers (R) in units of 1 register.	64 points
	Batch write		EW	45H, 57H	Writes extension file registers (R) in units of 1 register.	64 points
	Test (random write)		ET	45H, 54H	Specifies the extension file registers (R) in units of 1 register using block or device number and makes a random write.	10 points
	Monitor data registration		EM	45H, 4DH	Sets the extension file registers (R) device numbers to be monitored in units of 1 register.	20 points
	Monitor		ME	4DH, 45H	Monitors the extension file register after monitor data registration.	—

	PC CPUs with Which the Command can be Executed									PC CPU State			
	A0J 2H A1S	A1N A1	A2N A2 (S1)	A2A (S1)	A3N A3	A3A	A3H	A3M	A73	During STOP	During RUN		Reference Section
											SW22 ON	SW22 OFF	
													8.7.2
					o					o	o	o	8.7.3
													8.7.4
					o					o	o	x	8.7.5
													8.7.6
					o					o	o	x	8.7.7
					o					o	o	o	8.7.8
					o					o	o	o	
	o	x			o					o	o	o	8.8.4
	o	x			o					o	o	x	8.8.5
	o	x			o					o	o	x	8.8.8
	o	x			o					o	o	o	8.8.9
	o	x			o					o	o	o	

Table 3.3 Functions List When Using a Dedicated Protocol (Continued)

Function				Command: Symbol	Command: ASCII Code	Description		Number of Point Processed per Communications
Buffer memory	Batch read			CR	43H, 52H	Reads data from the AJ71C24 buffer memory.	Also usable for communications between the sequence program and the external devices when a multi-drop link is made.	64 words (128 bytes)
	Batch write			CW	43H, 57H	Writes data to the AJ71C24 buffer memory.		
Special function module	Batch read			TR	54H, 52H	Reads the contents of the special function module buffer memory.		64 words (128 bytes)
	Batch write			TW	54H, 57H	Writes data to the special function module buffer memory.		
Sequence Program	Batch read	Main	Other than T/C set value	MR	4DH, 52H	Reads main sequence programs.		64 steps
			T/C set value			Reads T/C set values used in main sequence programs.		64 points
		Sub	Other than T/C set value	SR	53H, 52H	Reads subsequence programs.		64 steps
			T/C set value			Reads T/C set values used in subsequence programs.		64 points
	Batch write	Main	Other than T/C set value	MW	4DH, 57H	Writes main sequence programs.		64 steps
			T/C set value			Writes T/C set values used in main sequence programs.		64 points
		Sub	Other than T/C set value	SW	53H, 57H	Writes subsequence programs.		64 steps
			T/C set value			Writes T/C set values used in subsequence programs.		64 points
Micro computer program	Batch read		Main	UR	55H, 52H	Reads main microcomputer programs.		128 bytes
			Sub	VR	56H, 52H	Reads submicrocomputer programs.		
	Batch write		Main	UW	55H, 57H	Writes main microcomputer programs.		
			Sun	VW	56H, 57H	Writes submicrocomputer programs.		
Comment	Batch read			KR	4BH, 52H	Reads comment data.		128 bytes
	Batch write			KW	4BH, 57H	Writes comment data.		
Parameter	Batch read			PR	50H, 52H	Reads parameters from PC CPU.		128 bytes
	Batch write			PW	50H, 57H	Writes parameters to PC CPU.		
	Analysis request			PS	50H, 53H	Causes PC CPU to acknowledge and check rewritten parameters.		—
PC CPU	Remote RUN			RR	52H, 52H	Request remote run/stop of PC CPU.		—
	Remote STOP			RS	52H, 53H			
	PC CPU read			PC	50H, 43H	Reads the type of PC CPU: A1N, A2N, A3N, A3H		
Global				GW	47H, 57H	Turns ON and OFF the global signal of the AJ71C24 loaded in each PC CPU system.		1 point
On-demand				—		Send request is initiated by a PC CPU. (Available in a 1:1 ratio system.)		Data length specified in the sequence program. (Max. 1760 words)
Loopback test				TT	54H, 54H	Echoes unchanged characters back to the computer.		254 characters

	PC CPUs with Which the Command can be Executed									PC CPU State			
	A0J 2H A1S	A1N A1	A2N A2 (S1)	A2A (S1)	A3N A3	A3A	A3H	A3M	A73	During STOP	During RUN		Reference Sections
											SW22 ON	SW22 OFF	
					o					o	o	o	8.9.2
													8.9.3
					o					o	o	o	8.10.3
					o					o	o	x	8.10.4
					o					o	o	o	8.12.4
			x				o			o	o	o	
					o					o	o *2	x	
					o					o	o	x	
			x				o			o	o *2	x	
			x				o			o	o	x	
		o		x	o	x		o		o	o	o	8.12.5
		x											
		o		x	o	x		o		o	o *2	x	
		x											
					o					o	o	o	8.12.6
					o					o	o	x	
					o					o	o	o	8.12.3
					o					o	x	x	
					o					o	x	x	
					o					o	o	o	8.11.2
					o					o	o	o	8.11.3
					o					o	o	o	8.13
					o					—	o	o	8.14
					o					o	o	o	8.15

*1: When the CPU modules other than A3H, A2A(S1), and A3A are used, devices X (input) are allocated with 2 inputs per device.

To include devices X in designated devices, set as follows:

((number of designated X devices x 2) + number of other designated devices) ≤ 40

If only devices X are designated, the number of inputs usable for one communications time is half the value mentioned in the table.

*2: Writing during a program run may be carried out if all the following conditions are met:

(This is different from the write during PC RUN with a MELSEC-A series peripheral device (e.g., A6GPP).)

(a) The PC CPU is type A3, A3N, A3H, A3M, A73 or A3A.

(b) The program is not the currently running program.

(includes subprograms called by the currently running main program)

(c) The PC CPU special relay is in the following states:

1) M9050 signal flow exchange contact.....OFF (A3CPU only)

2) M9051 (CHG instruction disable).....ON

POINT

When the AJ71C24 is used together with the A2ACPU (S1) or A3ACPU, use the commands in Table 3.4 to perform the following functions:

- Batch read/write, test, monitor data registration, and monitor of device memory
- Batch read/write of extension file registers by designating device numbers (continuous numbers)
- Batch read/write of extension comments

When the commands in Table 3.3 are used, the available functions and the range of devices which can be designated are limited to those available with the A3HCPU.

Accordingly, A2ACPU(S1) and A3ACPU external devices are not accessible.

(2) Functions available with the AnACPU dedicated commands

Table 3.4 Functions List When Using a Dedicated Protocol

Function			Commands: Symbol	Commands: ASCII Code	Description	Number of Point Processed per Communications	PC CPU State: During STOP	PC CPU State: During RUN: SW22 ON	PC CPU State: During RUN: SW22 OFF	Reference Sections
Device memory	Batch read	Bit units	JR	4AH, 52H	Reads bit devices (such as X, Y, M) in units of 1 device.	256 points	o	o	o	8.7.2
		Word units	QR	51H, 52H	Reads bit devices (such as X, Y, M) in units of 16 devices.	32 words (512 points)				8.7.3
					Reads word devices (such as D, R, T, C) in units of 1 device.	64 points				
	Batch write	Bit units	JW	4AH, 57H	Writes bit devices (such as X, Y, M) in units of 1 device.	160 points	o	o	x	8.7.4
		Word units	QW	51H, 57H	Writes bit devices (such as X, Y, M) in units of 16 devices.	10 words (160 points)				8.7.5
					Writes word devices (such as D, R, T, C) in units of 1 device.	64 points				
	Test (random write)	Bit units	JT	4AH, 54H	Specifies bit devices (such as X, Y, M) and device number in units of 1 device at random and sets/resets the device.	20 points	o	o	x	8.7.6
		Word units	QT	51H, 54H	Specifies bit devices (such as X, Y, M) and device number in units of 16 devices at random and sets/resets the device.	10 words (160 points)				8.7.7
					Specifies word devices (such as D, R, T, C) and device number in units of 1 device at random and sets/resets the device.	10 points				
	Monitor data registration	Bit units	JM	4AH, 4DH	Sets bit devices to be monitored (such as X, Y, M) in units of 1 device.	40 points	o	o	o	8.7.8
		Word units	QM	51H, 4DH	Sets bit devices to be monitored (such as X, Y, M) in units of 16 devices.	20 words (320 points)				
					Sets word devices to be monitored (such as D, R, T, C) in units of 1 device.	20 points				
	Monitor	Bit units	MJ	4DH, 4AH	Reads data from devices for which device data has been registered.	—	o	o	o	
		Word units	MQ	4DH, 51H						
Extension file register	Direct read	Word units	NR	4EH, 52H	Reads data in units of 1 device by designating the device numbers continuously regardless of the extension file register block numbers.	64 points	o	o	o	8.8.6
	Direct write	Word units	NW	4EH, 57H	Writes data in units of 1 device by designating the device numbers continuously regardless of the extension file register block numbers.	64 points	o	o	x	8.8.7
Extension comment	Batch read		DR	44H, 52H	Reads the extension comment data.	128 bytes	o	o	o	8.12.7
	Batch write		DW	44H, 57H	Writes the extension comment data.		o	o	x	

POINT

The commands given in Table 3.4 can be used when the AJ71C24 is used together with the A2ACPU(S1) or A3ACPU. The whole range of device memory is accessible using these commands.

For functions other than those listed in Table 3.4, use the commands given in Table 3.3.

3.3.2 Functions available in the no-protocol mode

(1) Functions in the no-protocol mode

Function	Command	Description	Number of Point Processed per Communications	PC CPU State			Reference Section
				During STOP	During RUN		
					SW22 ON	SW22 OFF	
Send (PC CPU → external device)	—	A PC CPU uses the TO instruction to output data written to an AJ71C24 buffer memory area in unchanged code to an external device.	127 words (default value). Can be changed with buffer size setting (see Sections 7.4.4 and 7.4.5.).	o	o	o	Section 9
Receive (External device → PC CPU)	—	A PC CPU uses the FROM instruction to read from an AJ71C24 buffer memory which was transmitted from an external device.					

(2) Receive completion by the completed code and by the completion data length

There are two ways to complete the data receive when an AJ71C24 is receiving data from an external device:

(a) Reading the received data using the receive completed code (receive of variable-length data)

When an AJ71C24 receives the receive completed code which is set in the buffer memory by the user from an external device, the AJ71C24 transmits a received data read request to the sequence program.

The sequence program, in response to the read request, reads the received data up to the receive completed code transmitted by the external device.

The user can freely set the receive completed code.

(b) Reading the received data using the receive-completion data length (receive of fixed-length data)

When an AJ71C24 receives data of a designated length which is set in the buffer memory by the user from an external device, the AJ71C24 transmits a received data read request to the sequence program.

The sequence program, in response to the read request, reads the received data of the designated length transmitted by the external device.

The receive-completion data length can be set within the buffer memory area allocated for the no-protocol receive.

POINTS

(1) The functions available with the no-protocol mode cannot be used together with the functions available with the bidirectional mode mentioned in Section 3.3.3. Select either mode using the mode setting switch (see Section 4.3.1)/switching the mode (see section 3.4) and by setting the bidirectional mode setting area in the special applications buffer memory area (see Sections 3.5 and 10.2).

(2) The receive-completed code and the receive-completion data length can be set and enabled at the same time. When both of them are enabled, the received data read request to the sequence program is made in response to whichever is received first by the AJ71C24.

3.3.3 Functions available in the bidirectional mode

(1) Functions in the bidirectional mode

Function	Command	Description	Number of Point Processed per Communications	PC CPU State			Reference Section
				During STOP	During RUN		
					SW22 ON	SW22 OFF	
Send (PC CPU → computer)	—	A PC CPU uses the TO instruction to output data written to the AJ71C24 buffer memory area in unchanged code to a computer. When the AJ71C24 receives the response message from a computer after data send the AJ71C24 transmits a send completed signal to the sequence program.	127 words (default value). Can be changed with the buffer size setting (see Sections 7.4.4 and 7.4.5.)	o	o	o	Section 10
Receive (Computer → PC CPU)	—	A PC CPU uses the FROM instruction to read data from the AJ71C24 buffer memory which was transmitted by a computer. When the AJ71C24 receives the data read completed signal from the sequence program, the AJ71C24 transmits a response message for the data receive to a computer.					

(2) Setting data length setting for data send

The length of the data to be transmitted between an AJ71C24 and a computer is set within the send message. (see Section 1.1.1 (2) (b)).

(a) When data is transmitted to a computer:

When the data to be transmitted to a computer is output from the sequence program to an AJ71C24, the data length is written to the buffer memory of the AJ71C24.

The AJ71C24 sets the data length to a send message and transmits it along with the data to a computer.

This allows the length of a send message to vary according to the content and kind of data to be transmitted.

(b) When data is received from a computer:

When an AJ71C24 receives data from a computer, the AJ71C24 writes the data length contained in the message to its buffer memory.

The sequence program reads the data length from the buffer memory to read all the received data.

POINT

The functions available with the bidirectional mode cannot be used together with the functions available with the no-protocol mode mentioned in Section 3.3.2. Select either mode using the mode setting switch (see Section 4.3.1)/switching the mode (see section 3.4) and by setting the bidirectional mode setting area in the special applications buffer memory area (see Sections 3.5 and 10.2).

3.3.4 Transmission error data read function

This function permits the sequence program to read error data when the error LEDs on the front panel of the module are lit and permits the sequence program to turn OFF an error LED which is lit. Section 7.3 gives details about sequence programs.

(1) Reading transmission error data

The display status of the error LEDs is stored in buffer memory. The sequence program can read this data to permit the PC CPU to execute error checking and interlocking with data communication sequence programs.

(2) Function to turn off error LEDs

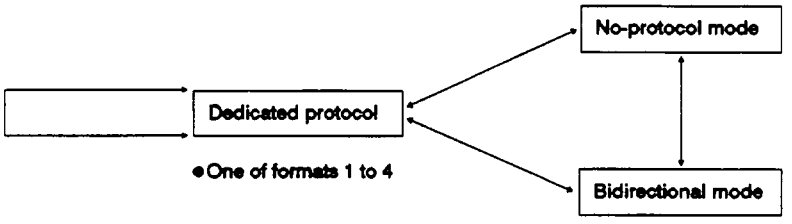
This function permits the sequence program to turn off error LEDs which are lit without resetting the PC CPU.

3.4 Mode Switching Function During AJ71C24 Operations

After an AJ71C24 started operations, AJ71C24's RS-232C/RS-422 interfaces can be switched to another mode.

(Mode switching when the AJ71C24 is online)

As shown below, this operation can be executed from an external device and a PC CPU.



3.4.1 Precautions when mode switching

This section gives the precautions to take when data communications is continued after switching the AJ71C24 mode during AJ71C24 operations.

(1) Settings between an external device and a PC CPU

Set the following items required to switch the mode between an external device and a PC CPU.

(a) Is the mode switched from an external device or a PC CPU?

(b) At what intervals are modes switched for each mode switching pattern?

Dedicated protocol (formats 1 to 4) mode:

Dedicated protocol (formats 1 to 4) mode

Dedicated protocol (formats 1 to 4) mode:

No-protocol/Bidirectional mode

No-protocol/Bidirectional mode:

Dedicated protocol (formats 1 to 4) mode

No-protocol mode : Bidirectional mode

Bidirectional mode : No-protocol mode

(c) How is an interlock provided for all connected devices?

- Method and message used to notify all connected stations of mode switching.
- Method and message used to notify all connected stations that mode switching has been completed.
- Device number and data description when PC CPU word devices are used.

(2) AJ71C24 operation contents when a request to switch the mode is accepted

AJ71C24 mode switching is requested by using the AJ71C24 buffer's mode switching designation area (address 119H).

When a mode switching request is accepted, the AJ71C24 executes the following operations:

(a) First turns OFF the AJ71C24 READY signal (Xn7).

(b) Initializes the AJ71C24 and starts it up (takes about six seconds).

During this operation, the following processings take place at the same time:

- Set data in the special applications area of the AJ71C24 buffer (addresses 100H to 11FH) is returned to the default state (except for address 119H).
- Received data (stored in the AJ71C24's buffer and the OS area) during data communications in the no-protocol/bidirectional mode is cleared.

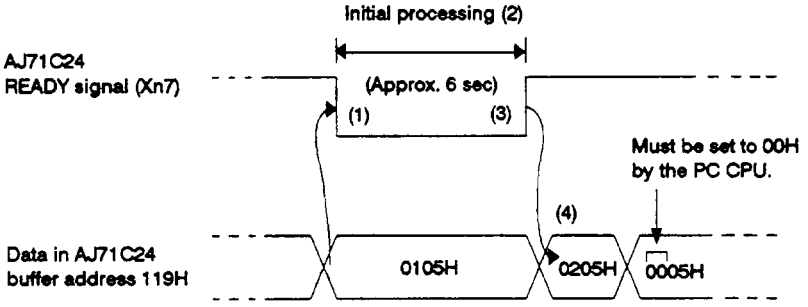
(c) Turns ON the AJ71C24 READY signal (Xn7).

(d) Switches the higher bytes in the AJ71C24 buffer's mode switching designation area (address 119H) from 01H to 02H.

The mode switching operation is completed.

Example:

When switching the RS-232C to the no-protocol mode and the RS-422 to the dedicated protocol (format 1) mode respectively



(3) Mode switching from an external device

(a) After switching the mode, an external device cannot be used to switch set data in the AJ71C24 buffer's special applications area.

If set data must be changed after switching the mode, write necessary data from the PC CPU (see Section 3.4.2 for the write timing).

When set data is not changed from the PC CPU, communicate by using the default data in the special applications area.

(b) When both the RS-232C and RS-422 are set to the no-protocol mode (mode switching designation data in 0109H), the mode cannot be switched by using an external device.

(This is because data cannot be written from the external device to the buffer's special applications area.)

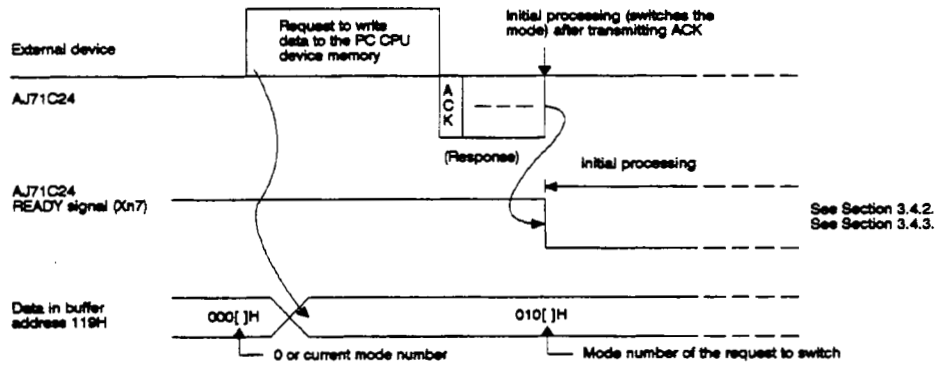
POINT

Mitsubishi recommends using a PC CPU for mode switching.

(4) Operations in response to a mode switching request when the data communications has not been completed

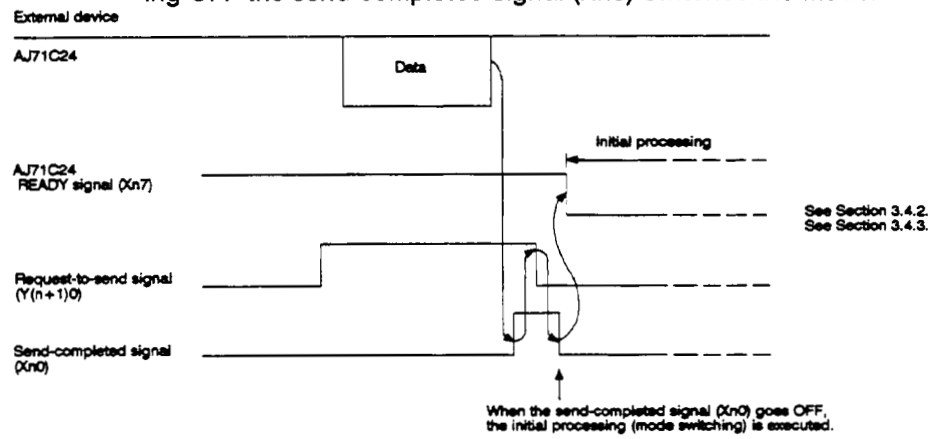
(a) When data communications in the dedicated protocol has not been completed, receiving a mode switch request will switch the mode after data communications has been completed (after transmitting data in area B (see Section 8.3)).

Example:



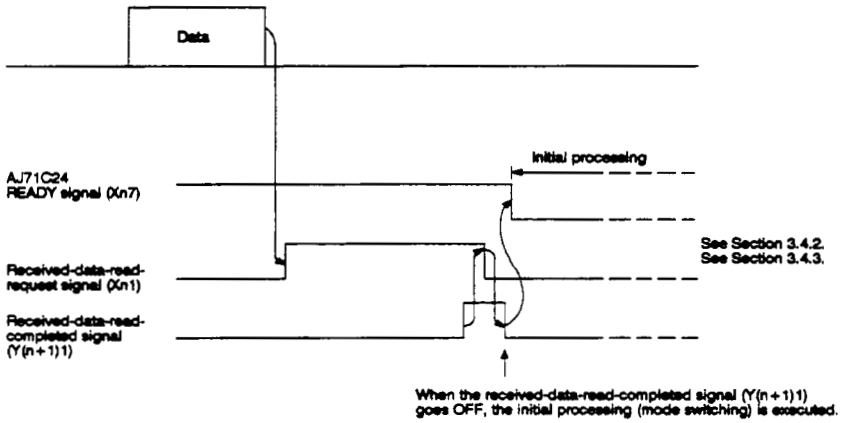
(b) When communicating data in the no-protocol/bidirectional modes, the AJ71C24 switches the mode under the following conditions:

1) When the AJ71C24 request-to-send signal (Y(n+1)0) is ON, turning OFF the send-completed signal (Xn0) switches the mode.



When this happens, if the request-to-send signal to the PC CPU has not been turned ON, the received data (stored in the AJ71C24 buffer and the OS area) will be cleared.

2) When the AJ71C24 received-data-read-request signal (Xn1) is ON, turning OFF the received-data-read-completed signal (Y(n+1)1) executes the mode switching.



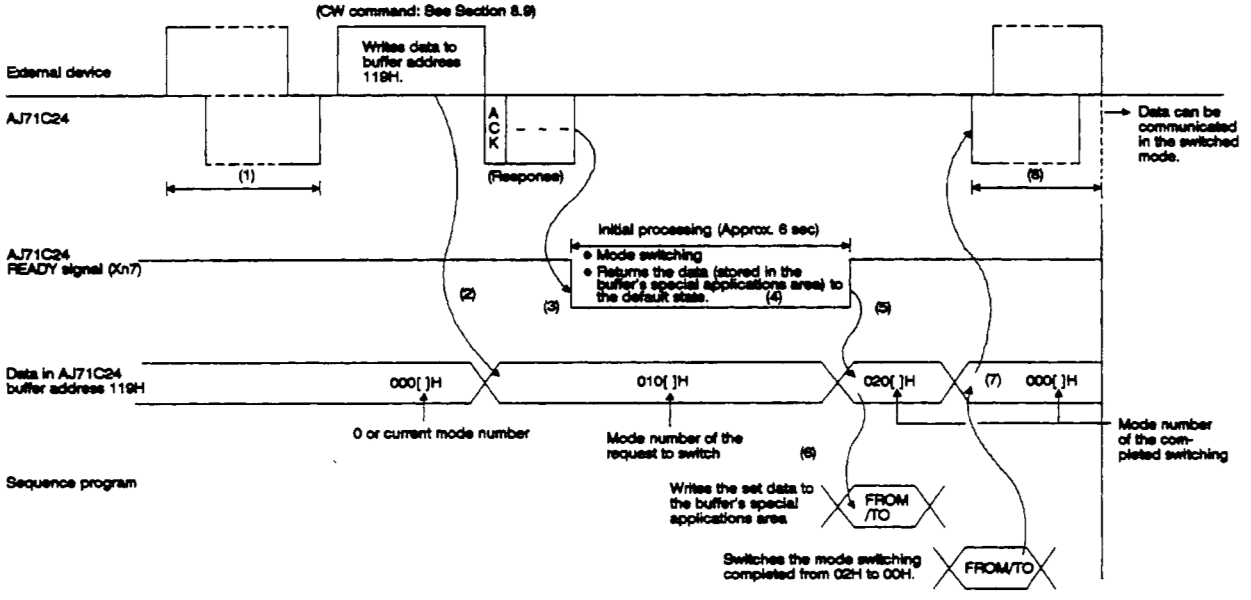
In this case, if the received data remains in the AJ71C24's OS area, that data will be cleared.

3.4.2 Procedure for switching the mode from an external device

Mode switching is executed via the interface of dedicated protocol (formats 1 to 4) using the CW command.

Before and after switching the mode, provide an interlock between sequence program operations and the mode switching operation (see Section 3.4.1(1)-3).

The mode switching procedure is shown below.

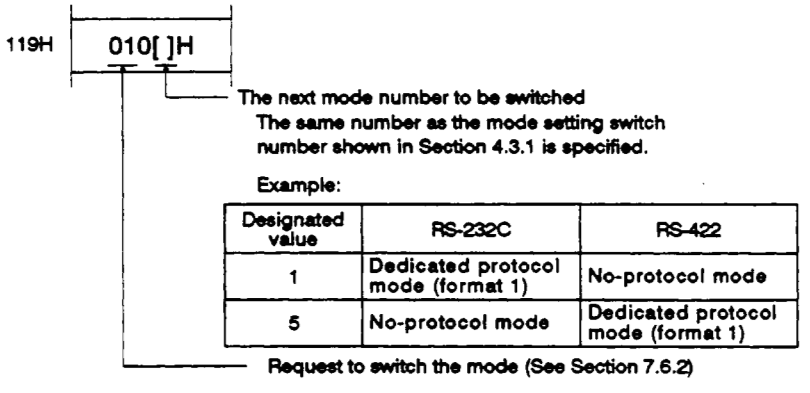

(CW command: See Section 8.9)
External device
Writes data to buffer address 119H.
AJ71C24
ACK
(1)
(Response)
(8)
Data can be communicated in the switched mode.
Initial processing (Approx. 6 sec)
AJ71C24 READY signal (Xn7)
• Mode switching
• Returns the data (stored in the buffer's special applications area) to the default state. (4)
(2)
(3)
(5)
Data in AJ71C24 buffer address 119H
000[ ]H
010[ ]H
020[ ]H
(7) 000[ ]H
0 or current mode number
Mode number of the request to switch (6)
Mode number of the completed switching
Sequence program
Writes the set data to the buffer's special applications area
FROM /TO
Switches the mode switching completed from 02H to 00H.
FROM/TO

This section describes steps (1) to (8) in the above figure.

(1) Before switching the mode, communicate the data to provide an interlock between the external device and the AJ71C24 (sequence program).

(This is because the mode switching conditions must be set for all connected devices.)

(2) By using the CW command, write the next mode number and the mode switching request from the external device to the mode switching designation area (address 119H).


119H
010[ ]H
The next mode number to be switched
The same number as the mode setting switch number shown in Section 4.3.1 is specified.
Example:
Request to switch the mode (See Section 7.6.2)

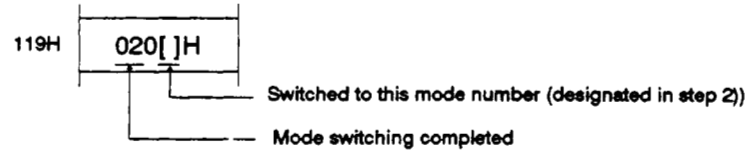
Designated value	RS-232C	RS-422
1	Dedicated protocol mode (format 1)	No-protocol mode
5	No-protocol mode	Dedicated protocol mode (format 1)

(3) The AJ71C24 completes the CW command execution normally and turns OFF its READY signal (Xn7) after transmitting the response message.

(4) The AJ71C24 starts switching the mode, executing the following operations:

- AJ71C24 initial processing
- Returning the data in the special applications area to the default state (except for the mode switching designation area (address 119H)).
- Clears received data.
- Mode switching
- Setting the switched-mode number to the mode setting state storage area (address 118H).

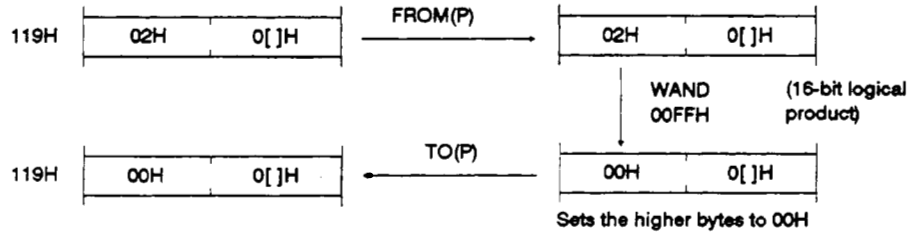
(5) After completing step 4), the AJ71C24 turns ON its READY signal, overwriting 02H to the higher bytes in the buffer's mode switching designation area.



(6) Write the set data (for communicating data in the switched mode in accordance with the higher bytes (changed to 02H)) to the AJ71C24 buffer's special applications area using a sequence program.

However, writing the set data is unnecessary if data can be communicated using the default data in the special applications area.

(7) Use a sequence program to read the data in the AJ71C24 buffer's mode switching designation area and write 00H to the higher bytes.



(8) After switching the mode, communicate data to provide an interlock between an external device and the AJ71C24.

(This operation notifies all connected devices that the special applications area setting has been completed and that data communications is enabled in the switched mode.)

POINT

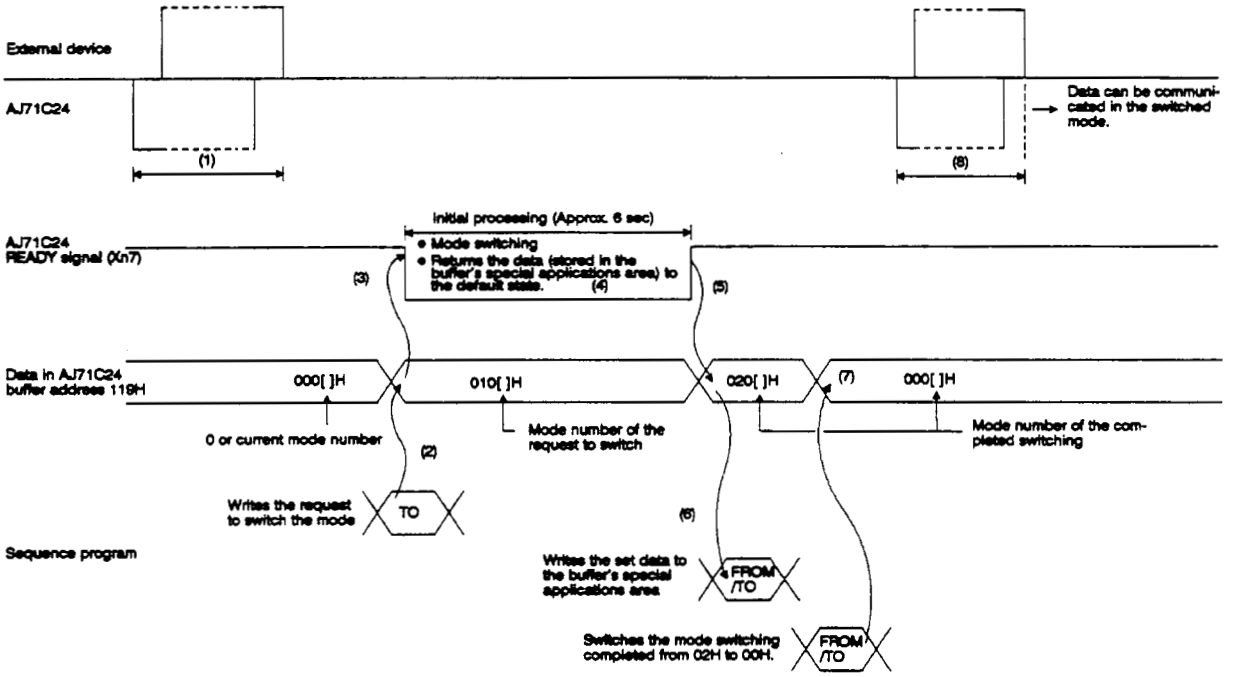
The AJ71C24 mode can be switched when the PC CPU is in the STOP state.

3.4.3 Procedure for switching the mode from a PC CPU

The mode is switched by using a FROM/TO instruction.

Before and after switching the mode, provide an interlock between sequence program operations and the mode switching operation (see Section 3.4.1(1)-3).

The mode switching procedure is shown below.

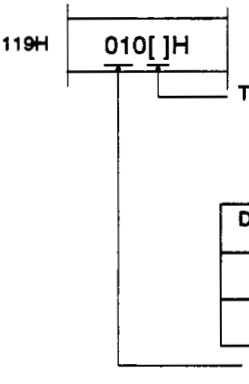


This section describes steps (1) to (8) shown in the above figure.

(1) Before switching the mode, communicate the data to provide an interlock between the external device and the AJ71C24 (sequence program).

(This is because the mode switching conditions must be set for all connected devices.)

(2) By using the CW command, write the next mode number and the mode switching request from the external device to the mode switching designation area (address 119H).


119H
010[ ]H
The next mode number to be switched
The same number as the mode setting switch number shown in Section 4.3.1 is specified.
Example:
Request to switch the mode (See Section 7.6.2)

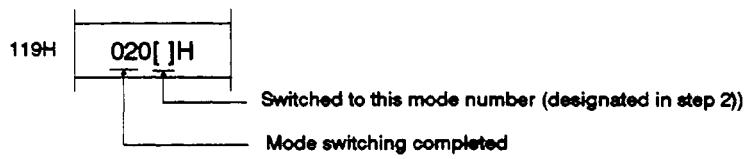
Designated value	RS-232C	RS-422
1	Dedicated protocol mode (format 1)	No-protocol mode
5	No-protocol mode	Dedicated protocol mode (format 1)

(3) The AJ71C24 turns OFF its READY signal (Xn7).

(4) The AJ71C24 starts switching the mode, executing the following operations:

- AJ71C24 initial processing
- Returning the data in the special applications area to the default state (except for the mode switching designation area (address 119H)).
- Clears received data.
- Mode switching
- Setting the switched-mode number to the mode setting status storage area (address 118H).

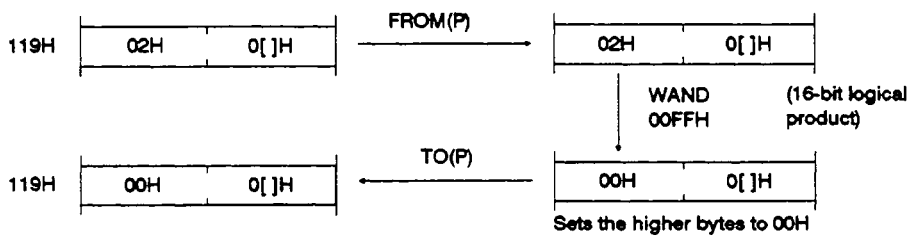
(5) After completing step 4, the AJ71C24 turns ON its READY signal, overwriting 02H to the higher bytes in the buffer's mode switching designation area.



(6) Write the set data (for communicating data in the switched mode in accordance with the higher bytes (switched to 02H)) to the AJ71C24 buffer's special applications area using the sequence program.

However, writing the set data is unnecessary if data can be communicated using the default data in the special applications area.

(7) Use the sequence program to read the data in the AJ71C24 buffer's mode switching designation area and write 00H to the higher bytes.



(8) After switching the mode, communicate data to provide an interlock between the external device and the AJ71C24.

(This operation notifies all connected devices that the special applications area setting has been completed and that data communications is enabled in the switched mode.)

3.5 Data Communications Transmission Control Function

This function uses the DC codes (DC1/DC3, DC2/DC4) or DTR/DSR signals to control data communications between the AJ71C24 and an external device. The AJ71C24 controls its data communications by using this function.

The following table shows the interfaces used and modes where transmission controls are enabled.

Transmission Control Function	Type of Control	Interface Used	Modes Where Transmission Controls are Valid			Remarks	
			No-Protocol	Bidirectional	Dedicated Protocol		
DTR/DSR controls	DTR control	RS-232C	O	—	—	The RS-422 is ignored.	DTR/DSR control or DC code control can be used.
	DSR control		O	O	O		
DC code control	DC1/DC3 transmission control	RS-232C RS-422	O	—	—	Controlled via both the RS-232C and RS-422.	
	DC1/DC3 receive control		O	O	O		
	DC2/DC4 transmission control		O	O	O		
	DC2/DC4 receive control		O	O	O		

O: Enabled (Transmission is controlled)
—: Disabled

3.5.1 Precautions when controlling transmission

This section gives the precautions to take when using the AJ71C24 transmission control function

(1) Deciding which items are required to control data communications between the external device and the PC CPU

(a) Is the transmission control function used? If so, which type of control is used?

(b) How is transmission controlled?

(c) If DC code control is used, which combination of codes is utilized?

(DC1 to DC4 codes can be switched.)

(2) Conditions for using the transmission control function

(a) Transmission cannot be controlled using both DTR/DSR signals and DC codes at the same time.

Select one type of control using the AJ71C24 buffer's transmission control designation area (address 11AH). (See item (3) below)

(b) Transmission is controlled via the RS-232 in the same way as via the RS-422.

(3) Settings when the transmission control function is/is not used

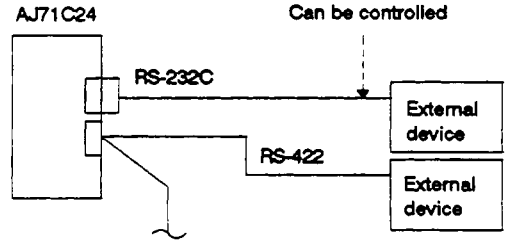
These settings specify whether or not the AJ71C24 transmission control function uses the AJ71C24 buffer's data communications control designation area (address 11AH).

These settings must be executed when power to the PC CPU is turned ON, the PC CPU is reset, or the AJ71C24 mode is switched.

Mode Number		1 to 4		5 to 8		9		A to D		See Section 4.3.1
Communications line		232C	422	232C	422	232C	422	232C	422	232C: RS-232C 422: RS-422
Mode		Dedicated protocol	No-protocol/Bidirectional	No-protocol/Bidirectional	Dedicated protocol	No-protocol		Dedicated protocol		
Data set for transmission control	DTR/DSR control	0000H (default)								See Section 7.7.1.
	DC code control	0101H, 0201H, or 0301H								
	When the transmission control function is not used	0001H								

(4) DTR/DSR control

Since there are no DTR/DSR signals in the RS-422 interface, when DTR/DSR control is designated, data cannot be communicated via the RS-422.



(5) DC code control

(a) DC1/DC3 transmission codes and DC1/DC3 receive codes can be controlled when executing full-duplex data communications between the AJ71C24 and its communicating device.

Data communications cannot be controlled using DC1/DC3 codes when executing half-duplex data communications.

(b) Avoid using DC1 to DC4 codes in the user's data.

If those codes must be used, take one of the following measures:

- Use DTR/DSR controls.
- Switch DC codes (see Section 7.7.2).
- Do not use the transmission control function.

POINT

When using a DC1/DC3 code to control data receive or DC2/DC4 code to control data receive, the AJ71C24 will execute the corresponding DC code control if the user's data (received from the external device) contains a DC code.

However, if the user's data (whose request to send was transmitted by a PC CPU) contains a DC code, that data will be transmitted.

(6) Handling DTR/DSR signals when DTR/DSR controls are not used

When DTR/DSR controls are not used, the AJ71C24 handles DTR/DSR signals as follows:

(a) DTR signal is normally ON.

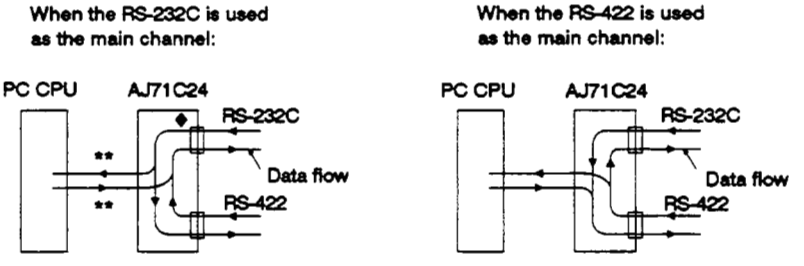
(b) The DSR signal ON/OFF state is ignored.

(7) Transmission control when the AJ71C24 mode number is 9 to D

When the AJ71C24 RS-232C and RS-422 are set to the same mode, the AJ71C24 controls data communications as shown below:

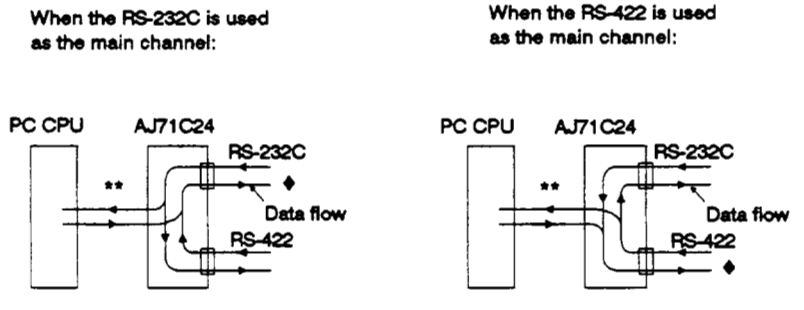
(mode number 9: no-protocol mode, modes A to D: dedicated protocol (formats 1 to 4))

(a) When DTR/DSR controls are executed



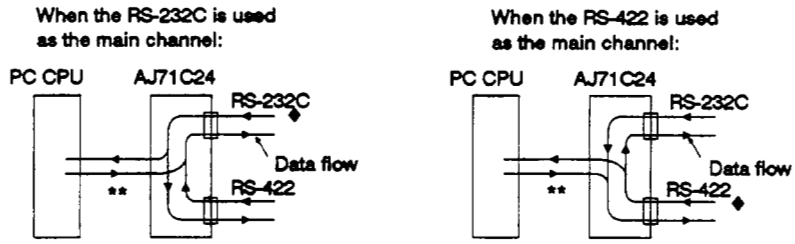
The ♦ mark indicates controlling send/receive data marked by **.

(b) When DC1/DC3 transmission control is executed



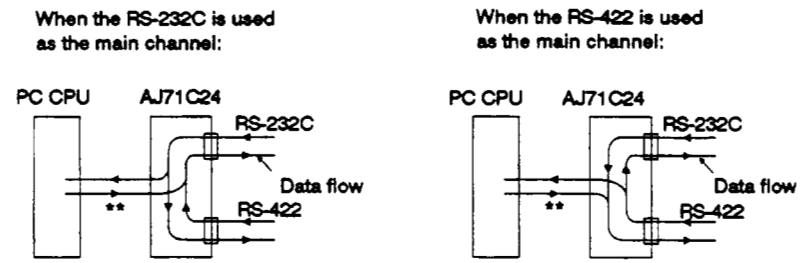
The ♦ mark indicates controlling receive data marked by **.

(c) When DC1/DC3 receive control is executed



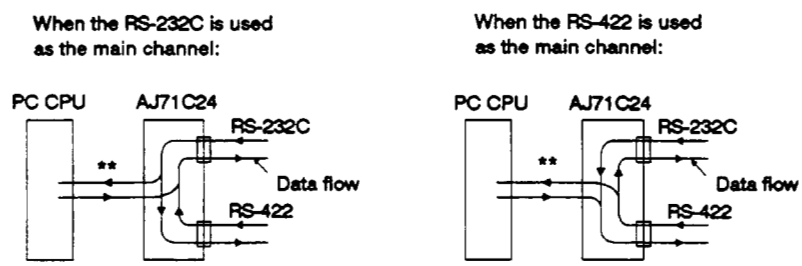
The ♦ mark indicates controlling send data marked by **.

(d) When DC2/DC4 transmission control is executed



Controlling send data marked by **.

(e) When DC2/DC4 receive control is executed



Controlling receive data marked by **.

3.5.2 DTR /DSR (ER/DR) control

This appendix explains DTR/DSR (ER/DR) control.

(1) Explanation of DTR/DSR control

DTR/DSR control enables and disables data communications with an external device via the AJ71C24 RS-232C by means of the DSR (DR) and DTR (ER) signals.

DTR/DSR control is not available for the RS-422.

(2) Receive data flow

Data received from an external device is stored in the AJ71C24 no-protocol receive buffer memory area via the OS memory area.

Under the following conditions, the AJ71C24 temporarily stores received data to its OS area. When transfer to the no-protocol receive buffer memory is enabled (read request signal Xn1 is OFF), data is transferred until the receive completed code is received, or until the fixed length of data has been transmitted.

Conditions:

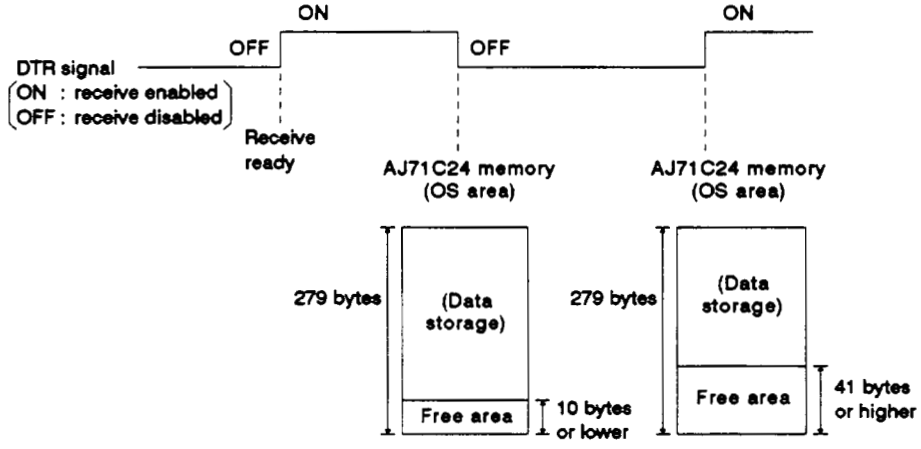
1) When there is too much data for the buffer memory because the received data length exceeds the no-protocol receive buffer memory area.

2) When data is transmitted from an external device before the PC CPU reads the data received previously.

(3) AJ71C24 DTR control

(a) The size of the receive data storage area of AJ71C24 OS area is 279 bytes. It turns the DTR signal ON and OFF as follows:

- less than 10 bytes storage area free : OFF
- more than 41 bytes storage area free : ON



(b) When received data is cleared as described in Section 9.5 (5), all data in the OS area is cleared at the same time as data in the no-protocol receive buffer memory area.

(c) When the above-mentioned OS area has no vacant area, receiving data causes an error, and the data is ignored until the OS area has enough vacant area.

When this happens, the 2-SIO LED goes ON (see Section 4.2.2).

(4) AJ71C24 DSR control

(a) When the AJ71C24 DSR signal is ON, if there is send data that data will be sent to an external device.

(b) When the AJ71C24 DSR signal is OFF, even if send data exists that data will not be sent to an external device.

3.5.3 DC1/DC3 transmission control

This section describes DC1/DC3 transmission control.

(1) What is DC1/DC3 transmission control?

When data communications is executed in the no-protocol mode, this notifies the external devices whether the AJ71C24 can or cannot receive data using the DC1/DC3 code.

(2) Received data flow and control operations

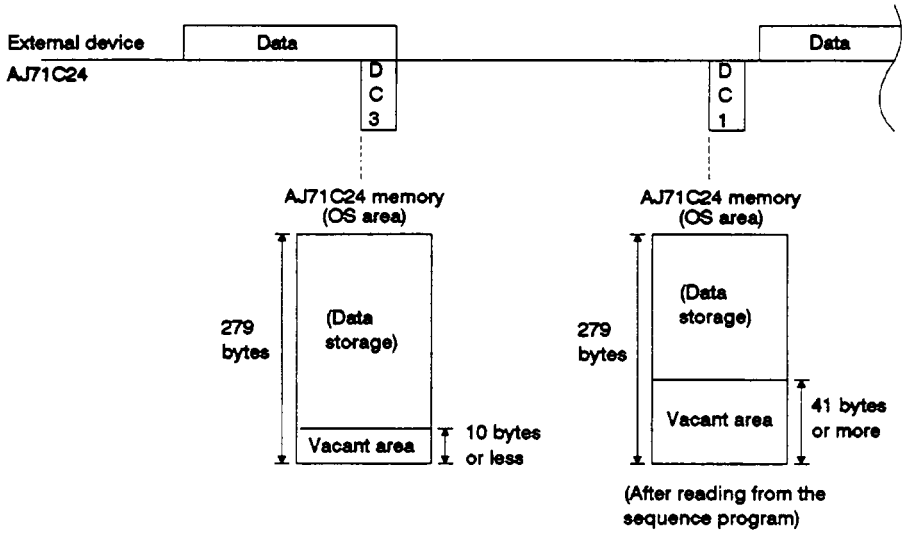
(a) Received data flows in the same way shown in Section 3.5.2(2). Data transmission is controlled in the same way as the DTR control shown in Section 3.5.2(3).

The AJ71C24 sends DC1 or DC3 to the external device without turning the DTR signal ON/OFF.

Section 3.5.2 gives details about DC1/DC3 transmission timing.

DTR signal state corresponds to the data transmission as shown below:

(DTR control) (DC1/DC3 transmission control)
DTR signal is OFF : DC3 transmission
DTR signal is ON : DC1 transmission



(b) Clear the received data as shown in Section 9.5. This operation is not only executed in the no-protocol receive buffer, but in the OS area as well.

(c) When the above-mentioned OS area has no vacant area, receiving data causes an error, and the data is ignored until the OS area has enough vacant area.

When this happens, the 2-SIO and 4-SIO LEDs go ON (see Section 4.2.2).

POINTS

(1) When power to the PC CPU is turned ON, the PC CPU is reset, or the mode is switched, DC1 code is not sent to the external device.

This is the same state as when DC1 has already been sent.

(2) DC1/DC3 codes to be sent can be changed.

Section 7.7.2 tells how to change codes.

3.5.4 DC1/DC3 receive control

This section describes DC1/DC3 receive control.

(1) What is DC1/DC3 receive control?

This function notifies the AJ71C24 whether or not an external device can receive data using DC1/DC3 codes.

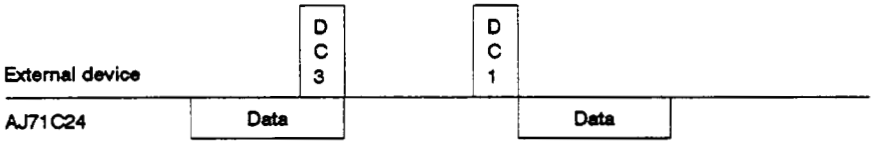
(2) Control operations

(a) Receiving DC3 code from an external device suspends AJ71C24 data send.

The received DC3 code is not available to the user.

(b) Receiving DC1 code from an external device resumes AJ71C24 data send.

The received DC1 code is not available to the user.



(c) After DC1 code is received, if another DC1 code is received, that code will be ignored and will be removed from the received data.

POINT

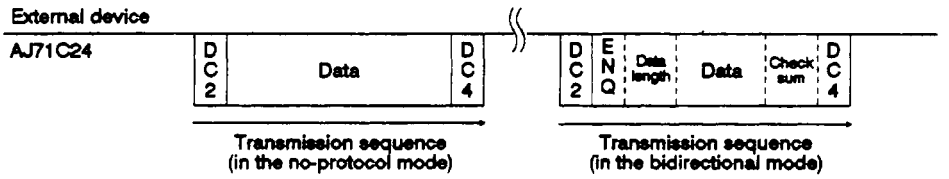
When power to the PC CPU is turned ON, the PC CPU is reset, or the mode is switched, even if a DC1 code is not transmitted, the state will be the same as when DC1 code has already been sent.

3.5.5 DC2/DC4 send control

This section describes DC2/DC4 send control.

(1) What is DC2/DC4 send control?

When data is sent from the AJ71C24 to an external device, the AJ71C24 adds DC2 and DC4 codes at the beginning and end of data respectively.



3.5.6 DC2/DC4 receive control

This section describes DC2/DC4 receive control.

(1) What is DC2/DC4 receive control?

By using DC2 and DC4 codes, this function determines the data range when the AJ71C24 receives data from an external device.

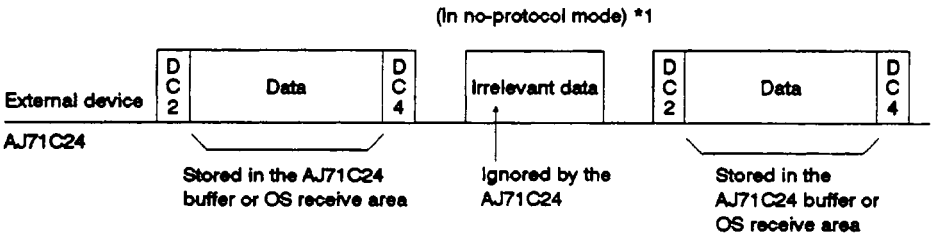
(2) Control operations

(a) When the AJ71C24 receives DC2 code from an external device, the AJ71C24 handles data in the range between DC2 and DC4 as valid data.

The received DC2 code is not available to the user.

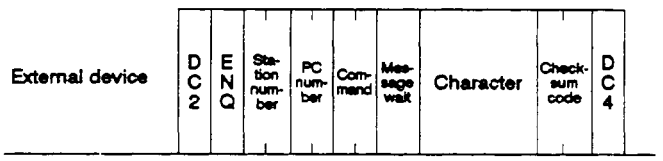
(b) When DC4 code is received from the external device, the AJ71C24 will ignore subsequent received data until another DC2 code is received.

The received DC4 code is not available to the user.



(c) After DC2 code is received, if another DC2 code is received, that code will be ignored, and will be removed from the received data.

*1 Message in dedicated protocol format 1



3.6 I/O Signals List for CPU

The I/O signals of the AJ71C24 for the PC CPU are listed below. The numbers (n number) appended to X and Y are determined by the installing position of the AJ71C24 and the number of I/O signals used by the I/O signal signals used by the I/O modules installed in front of the AJ71C24. (Example: Xn0 → X0 when the AJ71C24 is loaded in slot 0 of the main base unit)

(1) Input signals (AJ71C24 → PC CPU)

There are 16 input signals: Xn0 to XnF are turned ON/OFF by the AJ71C24.

Table 3.5 Input Signals List

Input Signal	Signal Name	Mode		Description	Reference Sections
		Dedicated protocol	No-protocol/ Bidirectional		
Xn0	Send completed	—	o	Turns ON when the send from the AJ71C24 to the external device is completed when Y(n+1)0 is turned ON. Turns OFF when Y(n+1)0 is turned OFF.	9.2, 10.2
Xn1	Received data read request	—	o	Turns ON when the completed code, fixed length data, or designated data length is received from the external device. Turns OFF when Y(n+1)1 is turned ON.	9.2, 10.2
Xn2	Global signal	o	—	Turns ON/OFF according to the message (factor number) when a global command is received from a computer.	8.13
Xn3	On-demand function operating	o	—	Turns ON when the on-demand transmission is executed according to the request from the sequence program. Turns OFF when the on-demand transmission is completed.	8.14
Xn4 to Xn6	AJ71C24 message sequence state	o	—	(1) Set values "1" to "8" of the mode setting switches (see Section 4.3.1) indicating the state of communications between the computer connected to the interface on the dedicated protocol side and the AJ71C24. Set values "A" to "D" of the mode setting switches indicating the state of communications between the computer connected to the interface on the main channel side (set with SW11, a transmission specification setting switch, see Section 4.3.2) and the AJ71C24. (2) Used by a sequence program to check communications status, etc.	—

Value	Xn6	Xn5	Xn4	Message Sequence State
0	OFF	OFF	OFF	AJ71C24 initializing after power ON or OFF using protocol 1 to 4
1	OFF	OFF	ON	Waiting for ENQ
2	OFF	ON	OFF	Received ENQ
3	OFF	ON	ON	Received station number (self)
4	ON	OFF	OFF	Waiting for response from PC after receiving all data
5	ON	OFF	ON	Waiting for message
6	ON	ON	OFF	Unused
7	ON	ON	ON	Unused

Input Signal	Signal Name	Mode		Description	Reference Sections
		Dedicated protocol	No-protocol/ Bidirectional		
Xn7	AJ71C24 READY signal	o	o	(1) Turns ON when the AJ71C24 becomes READY after the PC CPU is enabled. (Turns ON a few seconds after the power is turned ON.) Turns OFF when an error (which discontinues the AJ71C24's operation) occurs. (2) Used for the READY communications signal when the no-protocol mode, bidirectional mode, or the on-demand function of the dedicated protocol is used.	—
Xn8 to XnC	—	—	—	Unavailable	—
XnD	Watch dog timer error	o	o	Turns ON when the AJ71C24 watch dog timer error occurs. Remains OFF during normal operation.	11.2
XnE XnF	—	—	—	Unavailable	—

POINT

Y(Yn0 to YnF) corresponding to Xn0 to XnF may be used as internal relays.

(2) Output signals (PC CPU → AJ71C24)

There are 16 output signals: $Y_{(n+1)}0$ to $Y_{(n+1)}F$ are turned ON/OFF by the AJ71C24.

Table 3.6 Output Signals List

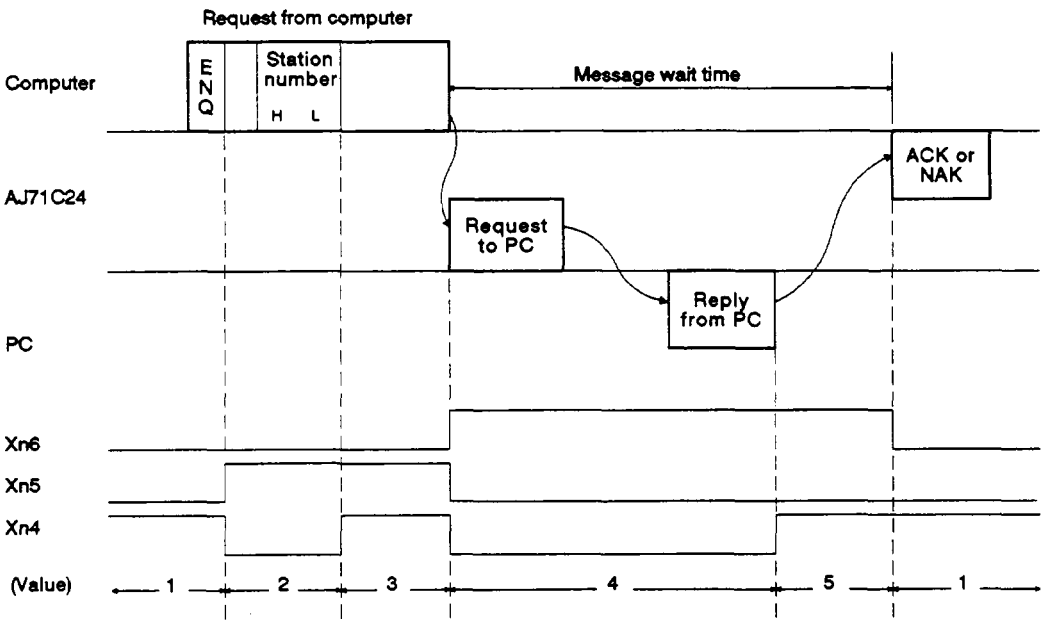
Output Signal	Signal Name	Mode		Description	Reference Sections
		Dedicated protocol	No-protocol/ Bidirectional		
$Y_{(n+1)}0$	Send request	–	o	When this signal is turned ON by the sequence program in the no-protocol mode/bidirectional mode, data written to the buffer memory is transmitted from the AJ71C24 to an external device. (After Xn0 is turned ON, $Y_{(n+1)}0$ is turned OFF.	9.2, 10.2
$Y_{(n+1)}1$	Received data read completed	–	o	This signal turns ON in the no-protocol mode/bidirectional mode, when the PC CPU has completed reading the data received from an external device. This data is stored in the AJ71C24 buffer memory. (After Xn1 is turned OFF, $Y_{(n+1)}1$ is turned OFF.	9.2, 10.2
$Y_{(n+1)}2$ to $Y_{(n+1)}F$	–	–	–	Reserved	–

IMPORTANT

$Y_{(n+1)}2$ to $Y_{(n+1)}F$ are reserved for system use only. AJ71C24 functions cannot be guaranteed if these signals are turned ON or OFF by a sequence program.

REMARK

Example: Use of input signals Xn4 to Xn6.



3.7 Buffer Memory Applications and Allocation

The term "buffer memory" used in this manual refers to a memory area of an AJ71C24 used to store the control and communications data which is transmitted between an external device (e.g., a computer) and a PC CPU.

The buffer memory can be accessed from the sequence program by using the FROM/TO instruction.

The buffer memory can be accessed from an external device by using the buffer memory read/write command (CR, CW) with dedicated protocols 1 to 4.

(1) Buffer memory applications

There are two types of buffer memory area. One area may be used freely by the user, but the other area has a special application.

(a) User area

There are four applications of the user area, which can be categorized as follows.

1) Data receive area in no-protocol mode/bidirectional mode

This area stores data transmitted from an external device in the no-protocol mode or bidirectional mode.

2) No-protocol mode/bidirectional mode data send area

This area stores data from the PC CPU to be transmitted to an external device.

3) On-demand data storage area

This area stores send data to be transmitted from the sequence program to an external device using the on-demand function.

4) Area when using buffer memory read/write commands

This area stores data when communication is made using protocols 1 to 4 for buffer memory read/write commands (CR,CW).

(b) Special applications area

The applications of this memory area are fixed. They are used to determine the data communications format and to change the allocation of the memory area for section (a) above.

When the power is turned ON, the PC CPU is reset or switching the mode, default values are written to this special applications area.

Default values can be changed to suit the purposes and applications of data transmission and the specifications of the external device. Section 7 gives details.

(2) Buffer memory allocation

The buffer memory consists of 16-bit addresses. The buffer memory has no back-up battery.

The buffer memory address names and values for each address are listed in the following table.

IMPORTANT

Buffer memory addresses 10EH, 11DH to 11FH are reserved for system use only. Data written to this area will prevent correct operation of the AJ71C24.

The following table shows the contents of the buffer memory allocation.

The memory areas which are used with the no-protocol mode or the bidirectional mode are listed as those to be used with the no-protocol mode.

The memory areas function the same way in either mode. When the bidirectional mode is required, see the following table, changing "no-protocol" to "bidirectional".

Table 3.7 Buffer Memory

Addresses	Buffer Memory Address Names			Default Values	Dedicated Protocol	No-Protocol	Bidirectional	(Reference Sections)
0H	User area (256 words)	Area for default	No-protocol send data length storage area	0 (No-protocol send area)	o *3	o	o	8.14, 9, 10
1H to 7FH			No-protocol send buffer memory area (Send data storage area)			o	o	
80H			No-protocol received data length storage area.	0 (No-protocol receive area)		Δ	Δ	
81H to FFH			No-protocol receive buffer memory area (Received data storage area)			Δ	Δ	
100H●	Area to specify receive completed code in no-protocol mode			0D0AH (CR, LF)	—	o	—	7.4.1
101H	Error LED display OFF state storage area			0	Δ	Δ	Δ	7.3.1
102H	Error LED turn OFF request area			0	o	o	o	7.3.2
103H●	Area to specify word or byte units in no-protocol mode			0 (words)	o *1	o	o	7.4.3
104H●	Area to specify head address of send buffer memory for no-protocol mode			0	—	o	o	7.4.4
105H●	Area to specify send buffer size for no-protocol mode			80H	—	o	o	
106H●	Area to specify head address of receive buffer memory for no-protocol mode			80H	—	o	o	7.4.5
107H●	Area to specify receive buffer size for no-protocol mode			80H	—	o	o	
108H●	Area to specify receive completion 1 on data length in no-protocol mode			127 (words)	—	o	—	7.4.2
109H	Area to specify head address of on-demand buffer memory			0	o	—	—	8.14
10AH	Area to specify on-demand buffer size			0	o	—	—	
10BH●	Area to specify RS-232C CD terminal check			0 (check CD terminal)	o	o	o	7.1
10CH	Storage area for on-demand errors			0	Δ	—	—	8.14
10DH	Receive data clear request area for no-protocol mode			0	—	o	Δ	9.5
10EH	System area (unavailable)			—	—	—	—	
10FH●	RS-232C communications mode setting area			0 (Full-duplex transmission)	o	o	o	7.2
110H●	Simultaneous send priority/non-priority setting area*2			0 (Priority)	o	o	o	
111H●	Send method setting area when transmission is resumed*2			0 (No retransmission)	o	o	o	
112H●	Bidirectional mode setting area			0 (No-protocol mode)	—	—	o	7.5
113H●	Time-out check time setting area			0 (Infinite)	—	—	o	
114H●	Simultaneous transmission data valid/invalid setting area			0 (Data valid)	—	—	o	
115H●	Check sum enable/disable setting area			0 (Check sum enabled)	—	—	o	
116H	Data send error storage area			0	—	—	—	10.2
117H	Data receive error storage area			0	—	—	—	

Addresses	Buffer Memory Address Names	Default Values	Dedicated Protocol	No-Protocol	Bidirectional	(Reference Sections)
118H	Mode setting state storage area	1H to DH *5	Δ	Δ	Δ	..... 7.6.1
119H	Mode change specification area	0 *6	o	o	o	..... 7.6.2
11AH●	Transmission control specification area (DTR/DSR control and DC code control)	0 (DTR/DSR control)	o	o	o	..... 7.7
11BH●	DC1/DC3 control code specification area	1311H	o	o	o	
11CH●	DC2/DC4 control code specification area	1412H	o	o	o	
11DH to 11FH	System area (Unusable)	—	—	—	—	
120H to 7FFH	User area (1760 words)	0	o *3	o *3	o *3	.... 8.14 9 10

*4

The o, Δ, and — symbols in the table indicate the following:

o: PC CPUs and computers can read/write from/to this area.

Δ: PC CPUs and computers can only read from this area.

—: PC CPUs and computers do not need to read/write from/to this area.

*1: The unit of the transmission (send/receive) data in the no-protocol mode or bidirectional mode or of the send data when the on-demand function of the dedicated protocol is used.

*2: Set this when the RS-232C interface is set to half-duplex communications.

*3: Areas should be allocated so that they do not overlap with each other when (a) data is transmitted in the no-protocol mode or bidirectional mode, or (b) when more than one function of data transmission using the on-demand function of the dedicated protocol is used.

*4: Change the default values marked by the dot symbol (●) attached to the right of the address only when the READY signal of the AJ71C24 is turned ON after the power is turned ON or the PC CPU is reset.

Or change the default values when the higher bytes of the buffer's mode switching designation area (address 119H) change into 02H after the AJ71C24 READY signal is turned ON by switching the mode of the AJ71C24.

*5 Values (1H to DH) that correspond to set values (1 to D) of the mode setting switch (see Section 4.3.1) are stored as default values.

*6 0 is stored before switching the mode.

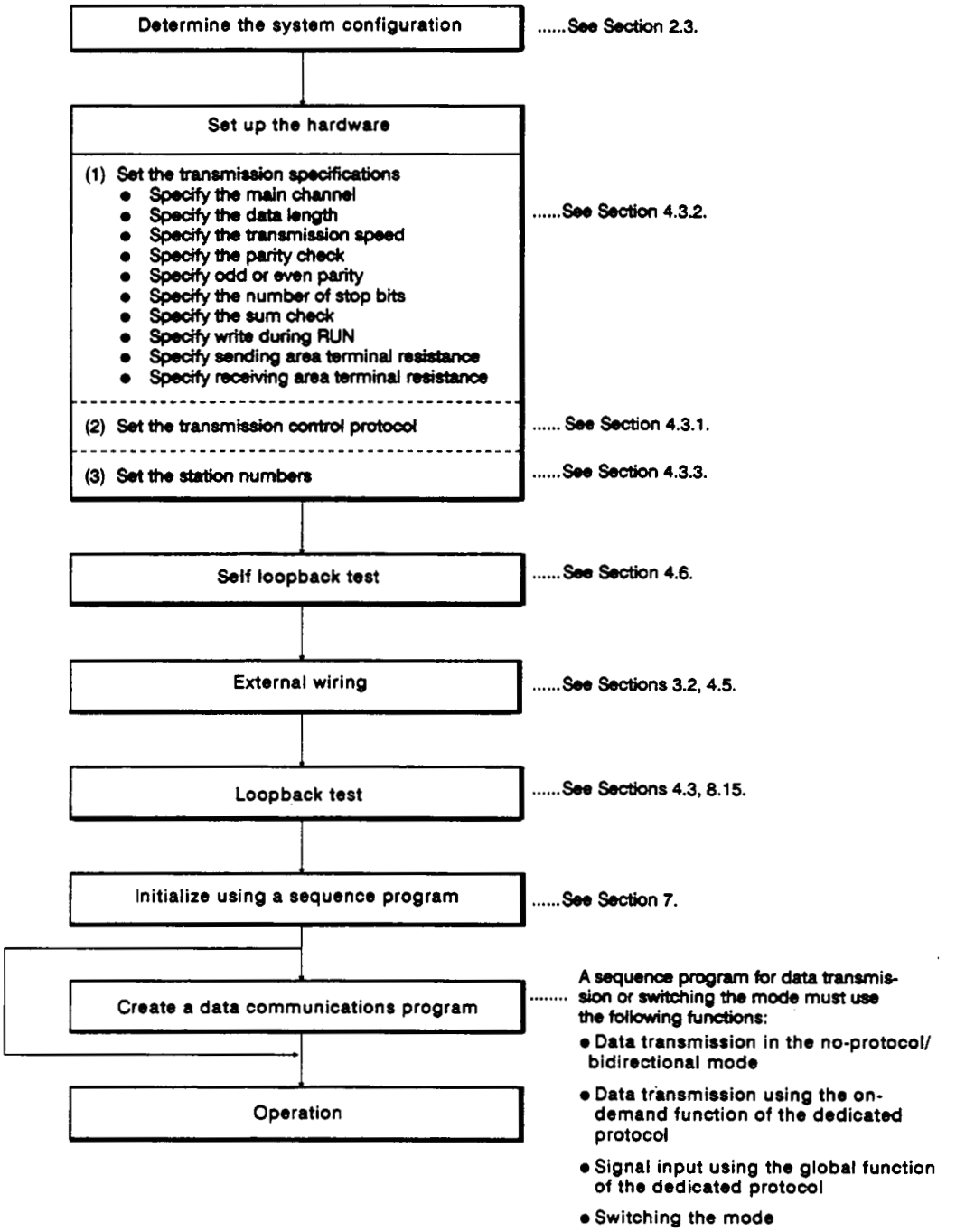
The values (1H to DH) of the mode number that correspond to the current mode are stored after switching the mode.

1H to DH correspond to the set values (1 to D) of the mode setting switch (see Section 4.3.1).

4. SETTINGS AND PROCEDURES BEFORE OPERATION

4.1 Settings and Procedures before Operation

The settings and procedures which have to be done before a system using the AJ71C24 can be started are described below.

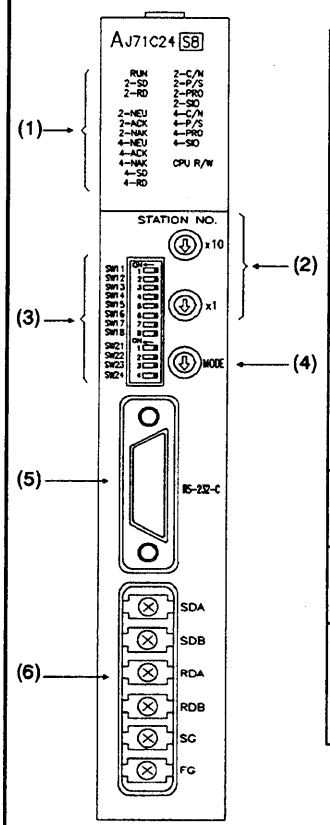

Determine the system configuration
.....See Section 2.3.
Set up the hardware
(1) Set the transmission specifications
• Specify the main channel
• Specify the data length
• Specify the transmission speed
• Specify the parity check
• Specify odd or even parity
• Specify the number of stop bits
• Specify the sum check
• Specify write during RUN
• Specify sending area terminal resistance
• Specify receiving area terminal resistance
.....See Section 4.3.2.
(2) Set the transmission control protocol
..... See Section 4.3.1.
(3) Set the station numbers
.....See Section 4.3.3.
Self loopback test
.....See Section 4.6.
External wiring
.....See Sections 3.2, 4.5.
Loopback test
.....See Sections 4.3, 8.15.
Initialize using a sequence program
.....See Section 7.
Create a data communications program
..... A sequence program for data transmission or switching the mode must use the following functions:
• Data transmission in the no-protocol/ bidirectional mode
• Data transmission using the on-demand function of the dedicated protocol
• Signal input using the global function of the dedicated protocol
• Switching the mode
Operation

REMARK

Appendix 12 contains the form sheet for recording the setting values of the AJ71C24.

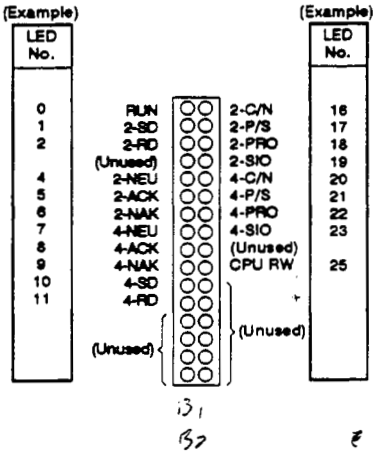
4.2 Nomenclature

4.2.1 Nomenclature



No.	Name	Description	Reference Sections
(1)	Indicator LEDs	Display the operating status, computer communications underway, and alarms.	4.2.2
(2)	Station number setting switches	Switch to set the station number in a computer link system. The station number may be set to any value which does not duplicate another station number. Setting range 0 to 31. (Factory-set to 0)	4.3.3
(3)	Transmission specification setting switches	Used to select RS-422/RS-232C, data bit, parity presence absence, stop bit, sum check, etc.	4.3.2
(4)	Mode setting switch	Switch for selecting transmission control protocol	4.3.1
(5)	RS-232C connector	RS-232C connector for linking an AJ71C24 with an external device	3.2.2 4.5.2
(6)	RS-422 terminal block	RS-422 terminal block for connecting an AJ71C24 with an external device or another AJ71C24. Terminal block screws are M4.	3.2.3 4.5.3 4.5.4

4.2.2 LED signals and displays



LED No.	LED	Meaning of LED Display	LED ON	LED OFF	Initial Status of LED
0	RUN	Normal run	Normal	Error	ON
1	2-SD	RS-232C transmitting	Flashes during data transmission		OFF
2	2-RD	RS-232C receiving	Flashes during data receive		OFF
4	2-NEU	RS-232C neutral	Transmission sequence initial state (waiting for ENQ)	ENQ received	*
5	2-ACK	RS-232C ACK	After sending ACK	After sending NAK	OFF
6	2-NAK	RS-232C NAK	After sending NAK	After sending ACK	OFF
7	4-NEU	RS-422 neutral	Transmission sequence initial state (waiting for ENQ)	ENQ received	*
8	4-ACK	RS-422 ACK	After sending ACK	After sending NAK	OFF
9	4-NAK	RS-422 NAK	After sending NAK	After sending ACK	OFF
10	4-SD	RS-422 transmission status	Flashes during data transmission		OFF
11	4-RD	RS-422 received data status	Flashes during data receive		OFF
16	2-C/N	Result of RS-232C and PC CPU communications	See (4) below	Normal	OFF
17	2-P/S	RS-232C parity/sum check errpr	Parity/sum check error	Normal	OFF
18	2-PRO	RS-232C protocol error	Communications protocol error	Normal	OFF
19	2-SIO	RS-232C SIO error	Overrun, framing error	Normal	OFF
20	4-C/N	Result of RS-422 and PC CPU communications	Parity/sum check error	See(4) below	OFF
21	4-P/S	RS-422 parity/sum check error	Parity/sum check error	Normal	OFF
22	4-PRO	RS-422 protocol error	Communication protocol error	Normal	OFF
23	4-SIO	RS-422 SIO error	Overrun, framing error	Normal	OFF
25	CPUR/W	Communications with PC CPU	Flashes during communications with PC CPU (ON at no communications)		ON

* varies according to the switch setting as shown in the following table.

Mode Setting / Main Channel Setting / LED No.	LED	1 to 4	5 to 8	9	A to D		F
		RS-232C RS-422	RS-232C RS-422	RS-232C RS-422	RS-232C	RS-422	RS232C RS-422
4	2-NEU	ON	OFF	OFF	ON	OFF	OFF
7	4-NEU	OFF	ON	OFF	OFF	ON	OFF

(1) LEDs 2-C/N to 4-SIO (LED Nos.16 to 23) above light when an error occurs. (Sections 3.5.2 and 3.5.3 also give details about 2-SIO and 4-SIO.)

The ON/OFF status of the LED Nos. 16 to 23 are stored in the buffer memory at address 101H. The status can be read using the PC CPU instruction which permits checking by a sequence program.

(Section 11 gives details about processing when an error is indicated.)

(2) After any LED 2-C/N to 4-SIO (LED Nos. 16 to 23) is ON, they remain ON even when the cause of the error is eliminated.

It is necessary to send a turn-off request to address 102H of the buffer memory using the sequence program TO instruction to turn OFF the LED.

(3) LEDs RUN to 4-RD (LED Nos. 0 to 11) and CPU R/W (LED No.25) above light corresponding to the relevant status.

(4) LEDs 2-C/N and 4-C/N (LED Nos. 16 and 20) above light in the following circumstances:

(a) When the AJ71C24 attempts to make an illegal access while the PC CPU is running (a write during program execution, for example).

(b) During abnormal PC CPU access.

(5) The "initial state" column indicates the status when the power is turned ON or the PC CPU is reset.

4.3 Settings

This section describes the setting methods and explains the settings of the transmission control protocol and communications specifications (data length, sum check, etc.).

After changing the settings, turn the PC CPU power supply OFF and back ON, or reset the PC CPU.

4.3.1 Setting the dedicated protocol, no-protocol mode, or bidirectional mode

(1) The method of setting the transmission control protocol and the meaning of the switch settings are described in the table below.

When the mode switch is set to "1" to "8" and the bidirectional mode setting area in the buffer memory is set to "1", the no-protocol mode in the following table changes to the bidirectional mode.

All mode settings in the following table are in the no-protocol mode.

Mode Setting Switch	Mode Setting Switch Number	Mode Settings		Notes
		RS-232C	RS-422	
MODE	0	Unusable		
	1	Protocol 1	No-protocol	For connection of computers to RS-232C and RS-422 individually, or for connection of a printer to the no-protocol interface. Both interfaces work independently.
	2	Protocol 2	No-protocol	
	3	Protocol 3	No-protocol	
	4	Protocol 4	No-protocol	
	5	No-protocol	Protocol 1	
	6	No-protocol	Protocol 2	
	7	No-protocol	Protocol 3	
	8	No-protocol	Protocol 4	
	9	No-protocol ←→	No-protocol	This mode is used to enable a no-protocol computer link with all devices connected to the RS-232C and RS-422 interfaces. Data transmitted by a computer can be received by all AJ71C24 modules. *1
	A	Protocol 1 ←→	Protocol 1	This mode is used to enable a dedicated protocol computer link with all devices connected to the RS-232C and RS-422 interfaces. Data transmitted by a computer can be received by the AJ71C24 designated by the send message. *1
	B	Protocol 2 ←→	Protocol 2	
	C	Protocol 3 ←→	Protocol 3	
	D	Protocol 4 ←→	Protocol 4	
	E	Unusable		
	F	For module test		RS-232C and RS-422 operate independently.

*1 : When the mode switch is set to "9" to "D", the RS-232C and the RS-422 interfaces operate as if interlocked with each other.

POINTS

Key points when setting modes.

(1) The RS-232C and RS-422 transmission specification protocols are identical. (See Section 4.3.2).

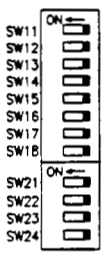
(2) To use the RS-232C and the RS-422 with a single mode, set the mode switch to "1" to "8".

(3) If there is any interface which is not connected to any external device when the mode setting is at "9" to "D", noise will come in through such an interface and normal communications cannot be done. In such a case, change the mode setting to "1" to "8".

(4) When the computers and the AJ71C24 modules are connected in an m:n multidrop link with the dedicated protocol, do not use protocol 3 ("7", "C").

(5) Sections 2.3.1 to 2.3.6 and 4.5.4 give the examples of settings with different system configurations.

4.3.2 Setting of transmission specifications, main channels, and terminal resistance

Setting of Switches	Setting Switches	Setting Items	Position of Setting Switch								Notes
			ON				OFF				
	SW11	Main channel settings	RS-422				RS-232C				Valid for modes A to D
	SW12	Data length	8 bits				7 bits				–
		Baud rate	300	600	1200	2400	4800	9600	19200	Unusable	–
	SW13	Transmission speed setting	OFF	ON	OFF	ON	OFF	ON	OFF	ON	
	SW14		OFF	OFF	ON	ON	OFF	OFF	ON	ON	
	SW15		OFF	OFF	OFF	OFF	ON	ON	ON	ON	
	SW16	Parity check	Enabled				Disabled				–
	SW17	Parity setting	Even				Odd				Valid only when parity check "enabled" is selected
	SW18	Stop bit	2 bits				1 bit				–
	SW21	Sum check	Enabled				Disabled				–
	SW22	Write during RUN	Enabled				Disabled				–
	SW23	Send area terminal resistance	Present				Absent				Valid only when RS-422 is used
	SW24	Receive area terminal resistance	Present				Absent				

(1) Main channel

The main channel in the above table refers to the interface to which the computer is connected. The main channel setting is valid only for modes A to D.

In other modes, the setting switch may be in the ON or OFF position.

(Section 4.5.4 gives the setting examples for different system configurations.)

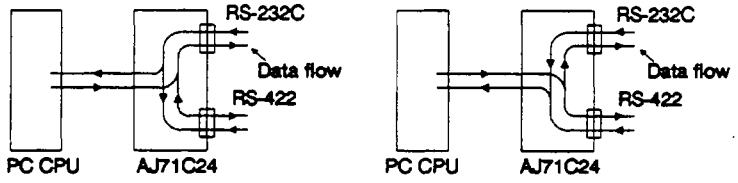
Setting the main channel defines data flow as shown below:

Data received through the main channel is automatically transmitted through the sub channel.

Data received through the sub channel is automatically transmitted through the main channel.

When the mode switch is set to "A" to "D", only the processing request commands, transmitted from other stations and received through the main channel of the self, are valid with the set mode.

The AJ71C24 executes the requested processing and transmits the result through the main channel.



RS-232C is set to the main channel

RS-422 is set to the main channel

(2) Transmission specifications

The RS-232C and RS-422 use the same transmission specifications. They cannot operate with two different transmission specifications settings.

Do not set the "unusable" baud rate setting (SW13, 14, and 15 ON).

If these switches are set, the RUN indicator LED (LED No. 0) is turned OFF and operation is not possible.

(3) Sum check

Set whether the sum check code is added or not added to the end of the message, when the computer link operates with the dedicated protocol.

Sections 8.4.1 to 8.4.4 and 8.4.5 (7) give the message structure and sum check code when the sum check setting is "Enabled".

(4) Write during RUN

Set whether a processing requested by the external device is executed or not executed by the PC CPU in the RUN state when the computer link operates with the dedicated protocol.

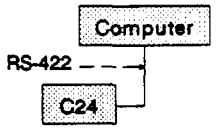
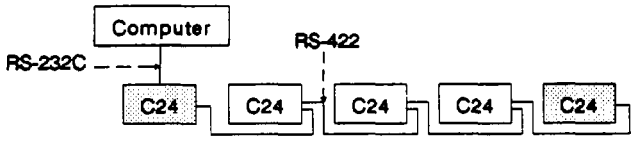
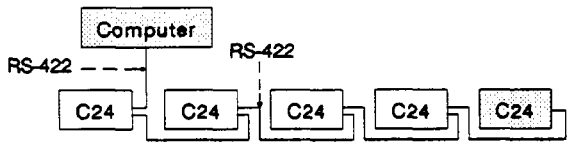
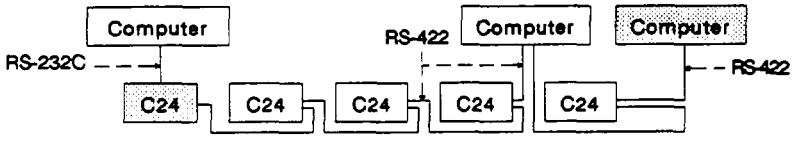
Section 3.3.1 gives the functions available with this setting.

(5) Terminal resistance at send and receive

When using the RS-422 cable, set the terminal resistance to "Present" at the stations connected to the both sides of the station which is linked with the RS-422 cable.

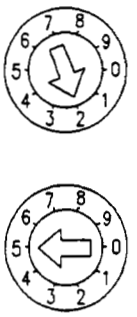
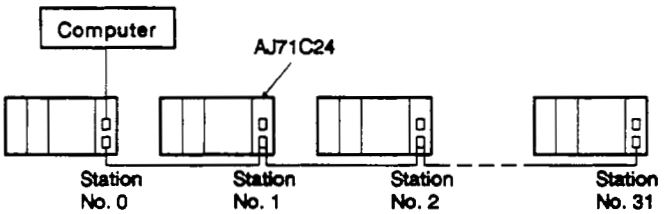
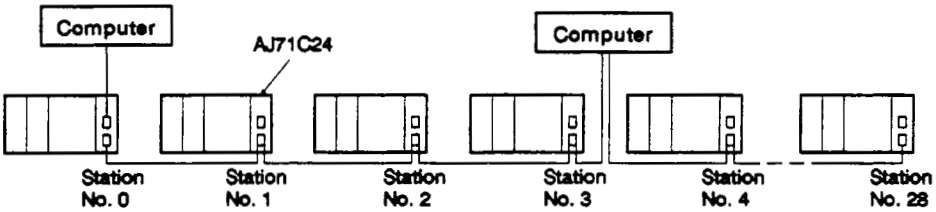
If this setting is not correct, normal computer link operations cannot be done.

The following chart shows examples of settings. Shaded boxes indicate the stations where terminal resistance needs to be set, and white boxes indicate the stations where terminal resistance need not be set. (Appendix 6 gives the settings to be done on the computers.)

Computer to PC CPU Ratio	System Configurations	Setting of AJ71C24 Where Terminal Resistance Needs to be Set	
		SW23	SW24
1 : 1		ON	ON
1 : n		ON	ON
		ON	ON
m : n		ON / OFF (Set either to ON)	OFF / ON (Set either to ON)

4.3.3 Station number setting

The station number is set on all AJ71C24s so that the computer knows which AJ71C24 to access in a 1 : n ratio computer link system.

Station Number Setting Switches	Description
	(1) Set the station number in the range 0 to 31. (Never set a station number to more than 32.) (2) Set the X10 switch to the number of tens in the station number. (3) Set the X1 switch to the number of units in the station number. (4) The station number may be set to any value which does not duplicate another station number. It is not necessary to consider the order of connection when viewed from the computer. Station numbers do not have to be sequential and may be skipped. (5) If the switches are set as shown on the left, the station number is 25. (1 : n ratio)  (m : n ratio) 

POINTS

(1) Use caution not to set a station number which duplicates another station number. This leads to destruction of transmission data and precludes correct data communications.

(2) When the computers and AJ71C24 modules are linked in an m : n ratio, set station numbers only for the AJ71C24s.

Set the station numbers for the computers to perform communications between them. Setting range is 128 (80H) to 159 (9FH). (See Section 6.2.1).

4.4 Loading and Installation

4.4.1 Handling instructions

(1) Protect the AJ71C24 and its terminal block impact.

(2) Do not touch or remove the printed circuit board from the case.

(3) Do not allow metal particles or wire offcuts to enter the AJ71C24.

(4) Tighten the module mounting and terminal screws as specified below.

Screw	Tightening Torque N·cm (kg·cm)(lb·inch)
RS-422 terminal block installation screws (M4)	78 (8)(6.93) to 137 (14)(12.13)
Module mounting screws (optional) (M4)	78 (8)(6.93) to 118 (12)(10.39)

(5) To load the AJ71C24 onto the base, press the AJ71C24 against the base so that the latch is securely locked. To unload the AJ71C24, push the latch and, after the latch is disengaged from the base, pull the AJ71C24 toward you.

4.4.2 Installation environment

Never install the system in the following environments:

(1) Locations where ambient temperature is outside the range 0 to 55°C (32 to 131°F).

(2) Locations where ambient humidity is outside the range of 10 to 90%RH.

(3) Locations where dew condensation takes place due to sudden temperature changes.

(4) Locations where there are corrosive gasses and combustible gasses.

(5) Locations where there is a high level of conductive powder, such as dust and iron filings, oil mist, salt, and organic solvent.

(6) Locations exposed to the direct rays of the sun.

(7) Locations where strong power and magnetic fields are generated.

(8) Locations where vibration and shock are directly transmitted to the main unit.

4.5 External Wiring

4.5.1 Precautions during wiring

External wiring which is resistant to external noise effects is a prerequisite for reliable AJ71C24 operations (full use of all available functions).

When doing external wiring of the AJ71C24, the following precautions must be taken:

(1) Keep main circuit wiring, high-voltage wiring, and other load-carrying wiring outside the PC CPU separate from AJ71C24 wiring. Never bundle them together. This prevents noise and surge-induction effects.

(2) Ground the shield of shielded wires and cables at only one point.

(3) The RS-422 terminal has M4 screw connectors. Fasten suitably-sized crimped terminals to the ends of the cables before connecting the cables to the terminals.

4.5.2 Connecting the RS-232C connectors

Precautions and examples of connections to an RS-232C connector is shown in the diagram below.

(1) Precautions during connections

(a) If the FG and SG terminals are connected inside a device connected to the RS-232C connector, do not use terminal No. 1 of the RS-232C connector of the AJ71C24.

(b) If half-duplex transmission (see Section 7.2 for the setting method) is used, perform wiring so that the CD signal of the AJ71C24 can be controlled by the external device.

Also, set the AJ71C24 to execute the CD terminal check (see Section 7.1).

Section 5.4 gives the ON/OFF timing control of the CD signal of the AJ71C24 using the external device.

(2) Examples

(a) Connections to a device which can turn the CD terminal signal ON (for full-/half-duplex transmissions)

AJ71C24		Cable Connections and Signal Directions	Computer
Signal Names	Pin Numbers		Signal Names
FG	1		FG
SD(TXD)	2		SD(TXD)
RD(RXD)	3		RD(RXD)
RS	4		RS
CS(CTS)	5		CS(CTS)
DSR(DR)	6		DSR(DR)
SG	7		SG
CD	8		CD
DTR(ER)	20		DTR(ER)

(b) Connections to a device which cannot turn the CD terminal signal ON (for full-duplex transmission)

1) When wired as in step (a) above, disable the RS-232C CD terminal check.

2) If the RS-232C CD terminal check function is enabled, wire the connectors as shown below.

AJ71C24		Cable Connections and Signal Directions	Computer
Signal Names	Pin Numbers		Signal Names
FG	1		FG
SD(TXD)	2		SD(TXD)
RD(RXD)	3		RD(RXD)
RS	4		RS
CS(CTS)	5		CS(CTS)
DSR(DR)	6		DSR(DR)
SG	7		SG
CD	8		CD
DTR(ER)	20		DTR(ER)

4.5.3 Connecting the RS-422 connectors

When connecting to an RS-422 connector, the following precautions must be taken. Connection examples are given in the diagram below.

(1) Precautions during connections

(a) To transmit FG and SG signals of the AJ71C24 to an external device, perform connections conforming to the specifications of the external device.

(b) The following example uses a 1:1 connection ratio between a computer and an AJ71C24.

Section 4.5.4 explains 1:n ("n" is up to 32) and m:n connection ratios (total of "m" and "n" is a maximum of 32) between computers and AJ71C24 modules.

(2) Example

AJ71C24 Signal Names	Cable Connections and Signal Directions	Computer Signal Names	Description
SDA		RDA	Receive data
SDB		RDB	Receive data
RDA		SDA	Send data
RDB		SDB	Send data
		RSA	Request to send
		RSB	Request to send
		CSA	Clear to send
		CSB	Clear to send
SG		SG	Signal ground
FG		FG	Frame ground

*1: Section 3.2.3 gives the signal assignment of the RS-422 terminal on the AJ71C24.

4.5.4 Connecting a multidrop link and setting modes and terminal resistance

The following gives an example of the multidrop link which consists of computers and AJ71C24 modules.

Sections 4.5.2 and 4.5.3 explain the connection of the signal cables which are not shown in the figure.

(SW23: [ ], SW24: [ ]) shown above the AJ71C24 indicate the terminal resistance settings.

(Mode: [ ] to [ ], Main:[ ]) shown below the AJ71C24 indicate the ranges of the mode setting switches and the interface setting with the main channel setting switch (only for related stations) when a multidrop link is constructed.

Values in ( ) on the top row are for the dedicated protocol. Those on the bottom row are for the no-protocol mode.

Mode: [ ] to [ ] .... Setting range of the mode setting switch for that station (see Section 4.3.1).

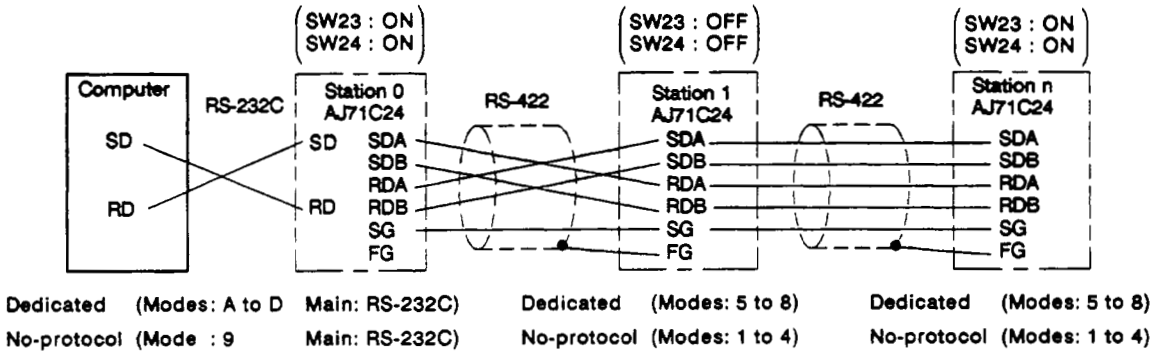
Main: [ ] .... The interface on the main channel setting of that station (see Section 4.3.2). Only those for related stations are shown.

REMARK

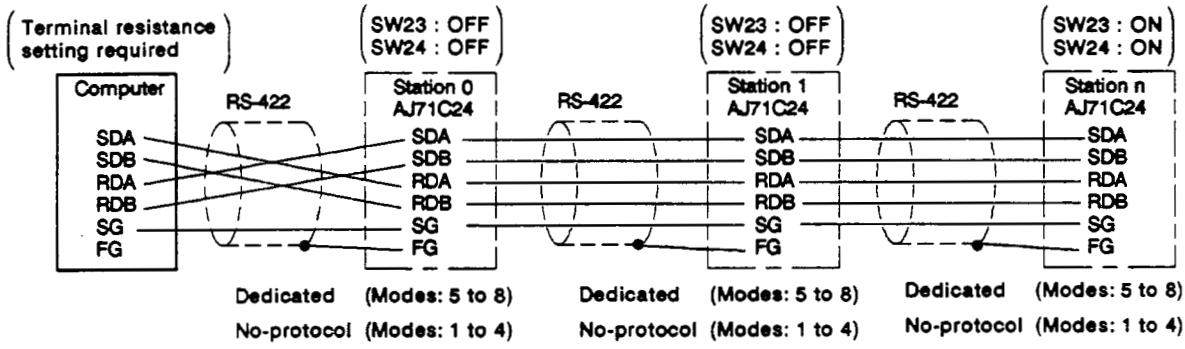
Set the terminal resistance of the stations which are connected to both ends of the RS-422 line to "Enable" when a multidrop link is constructed.

(1) 1 : n connection ratio

(a) A computer and station 0 AJ71C24 are connected through the RS-232C port:

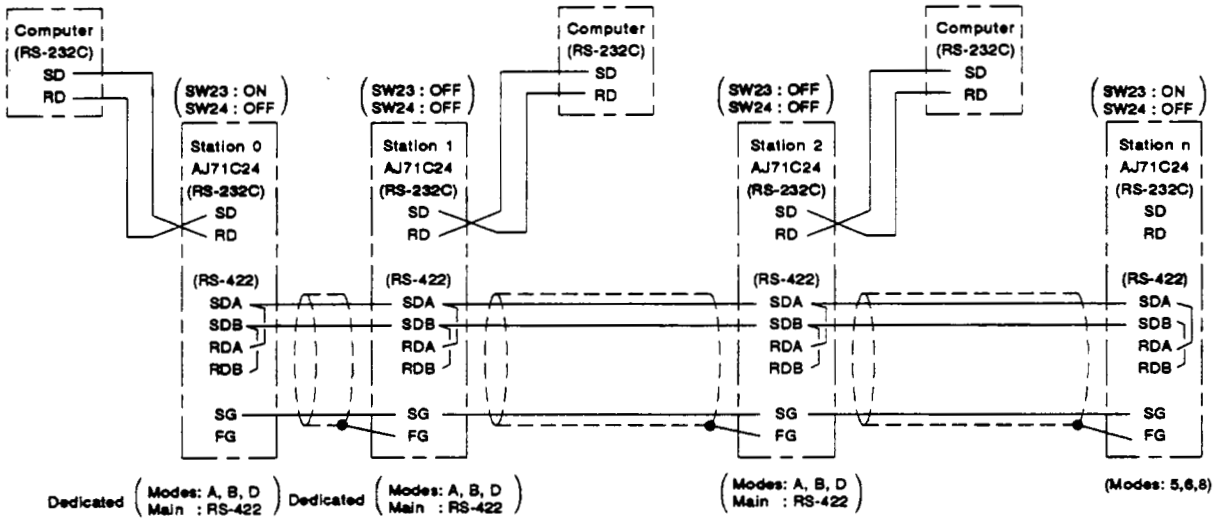


(b) A computer and station 0 AJ71C24 are connected through the RS-422 port:

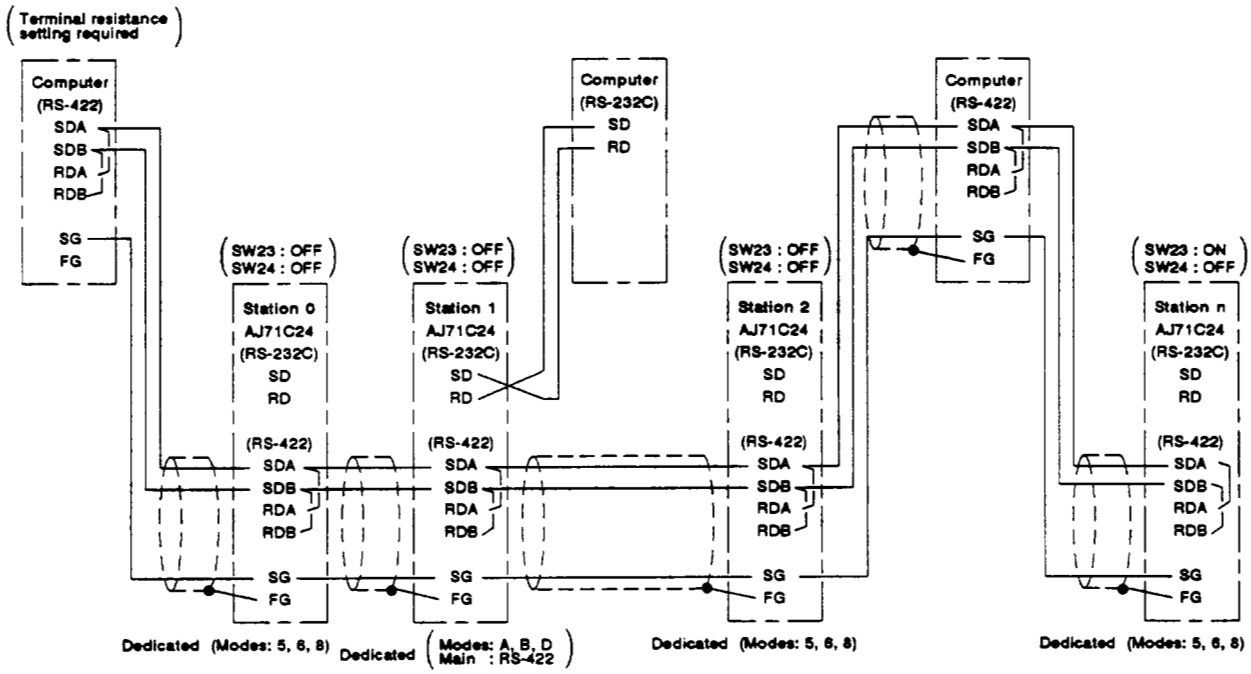


(2) m:n connection ratio

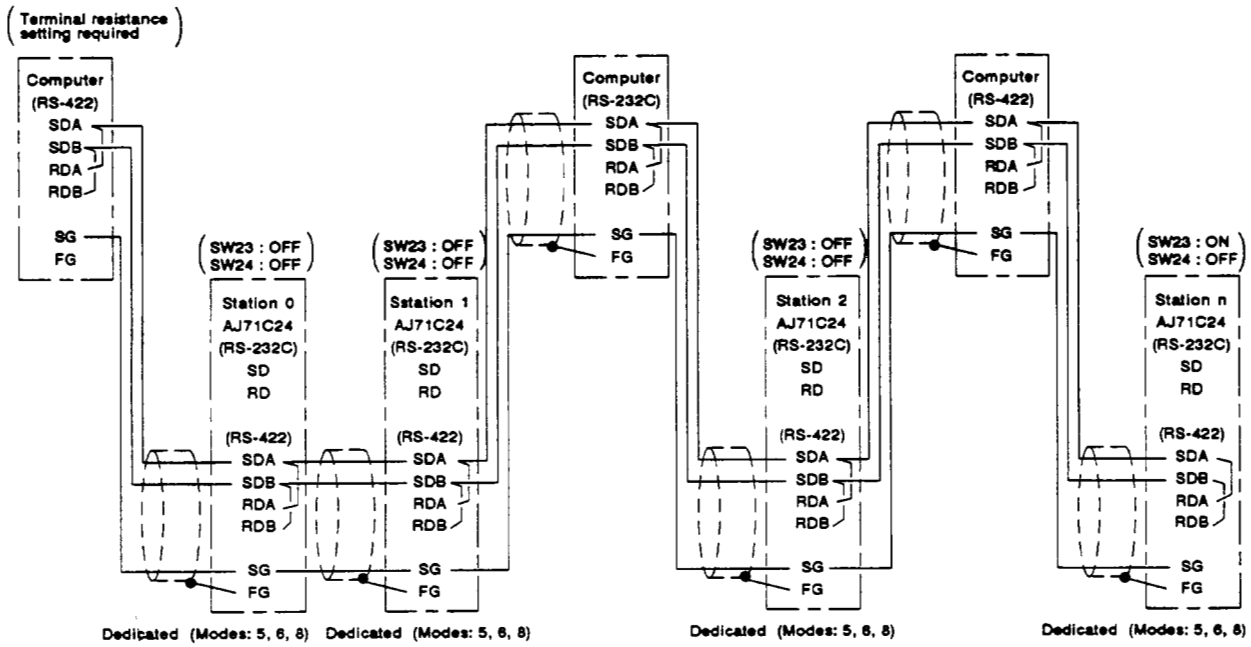
(a) The computer and the AJ71C24 are connected through the RS-232C, and the AJ71C24 modules are connected through the RS-422.



(b) The computer and the AJ71C24 are connected through the RS-232C and RS-422, and the AJ71C24 modules are connected through the RS-422.



(c) The computer and the AJ71C24 are connected through the RS-422.



4.6 Self-loopback Test

The self-loopback test function is used (when the AJ71C24 is not connected to the computer) to check that the AJ7C24 module is operating normally. This function is selected by setting the mode setting switch to "F".

4.6.1 Procedure to carry out the self-loopback test

The procedure to carry out the self-loopback test is as follows:

Step 1 Connect the cables

Connect cables to the RS-232C and RS-422 connectors as shown below.

RS-232C Cable Connections

AJ71C24		Cable Connections
Signal names	Pin number	
FG	1	
SD	2	
RD	3	
RS	4	
CS	5	
DSR	6	
SG	7	
CD	8	
DTR	20	

RS-422 Cable Connections

AJ71C24	Cable Connections
Signal Names	
SDA	
SDB	
RDA	
RDB	
SG	
FG	

Step 2 Set the mode setting switch

Set the mode setting switch to "F" to select the self-loopback test. (Section 4.3.1 tells details of how to set this switch.)

Step 3 Execute the self-loopback test

(1) Turn the PC CPU power supply ON or reset the PC CPU.

The test starts automatically when the AJ71C24 READY signal turns ON. The READY signal turns ON a few seconds after the power supply is turned ON or the PC CPU is reset.

(2) Check sequence

Checks are executed out in the following order:

1) PC CPU communications check

2) RS-232C communications check

3) RS-422 communications check

The checks are then repeated. The checks are completed within one second. The checks are executed automatically by the AJ71C24.

(3) Check the LED display status, as described in Section 4.6.2.

Normal : Follow procedure (4) to end the test.

Error : Correct the error and repeat the self-loopback test

(4) When checks are completed:

1) Turn the power supply OFF.

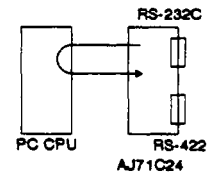
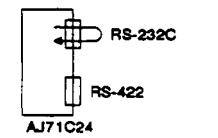
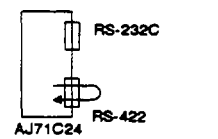
2) Disconnect the cables. Connect the cables to link with the computers.

3) Change the setting of the mode setting switch. ("1" to "D")

POINT

When the A2A(S1) or A3ACPU is used, up to 6 AJ71C24 modules can be connected to each PC CPU. When other types of PC CPUs are used, 1 or 2 AJ71C24 modules can be loaded to each PC CPU. However, do not execute the self-loopback test with both modules simultaneously (this will result in a PC CPU communications check error).

4.6.2 Self-loopback test operations

Check Items	Check Descriptions	Normal Indicator LED		Error Indicator LED		Information Flow
PC CPU communication check	After writing data to special data register D9072, the AJ71C24 reads and verifies it. If the data matches, it is changed and the procedure is repeated. If data does not match, an error is indicated.	2-C/N (LED No. 16)	OFF	2-C/N (LED No. 16)	ON	
		PC CPU R/W (LED No. 25)	Flashing			
RS-232C communications check	Checks data sent from RS-232C connector. If normal, AJ71C24 changes data and the procedure is repeated. If not normal, an error is indicated. An error is indicated if no cable is connected.	2-SIO (LED No. 19)	OFF	2-SIO (LED No. 19)	ON	
		2-SD (LED No. 1)	Flashing			
		2-RD (LED No. 2)				
RS-422 communications check	Checks data sent from RS-422 connector. If normal, AJ71C24 changes data and the procedure is repeated. If not normal, an error is indicated. An error is indicated if no cable is connected.	4-SIO (LED No. 23)	OFF	4-SIO (LED No. 23)	ON	
		4-SD (LED No. 10)	Flashing			
		4-RD (LED No. 11)				

*The test continues even if an error occurred with a checking item.

4.7 Loopback Test

The loopback test checks the correctness of data communications between the computer and the AJ71C24 using the dedicated command (TT) with the dedicated protocols 1 to 4.

The procedure to execute the loopback test is as follows:

Step 1 Connect the computer and AJ71C24

Connect the cable between the computer and AJ71C24 as described in Section 4.5.

Step 2 Mode switch settings

Set the mode switch to "1" to "D" to set the testing interface for the dedicated protocol. (Section 4.3.1 gives detail of the setting method.)

Step 3 PC CPU start-up

Turn the power to the PC CPU ON or reset the PC CPU. The AJ71C24 ready signal turns ON (ready for operation), after which the loopback test can be executed.

(The ready signal turns ON at a few seconds after the AJ71C24 is turned ON or reset.)

Step 4 Execute the loopback test command

(1) Create a program to be tested and transmit the command and data to the AJ71C24.

Section 8.4 gives the message structure of formats 1 to 4, and Section 8.15 gives the loopback command (TT).

(2) The AJ71C24 transmits the unchanged data back to the computer.

Step 5 Computer consistency check

(1) Check at the computer if data transmitted from the computer to the AJ71C24 is identical with the data transmitted back from the AJ71C24 to the computer.

Identical data indicates that the communication between the computer and AJ71C24 is normal.

If the data transmitted from the computer to the AJ71C24 and the data transmitted back from the AJ71C24 to the computer are not identical, the transmission specification settings probably do not match or the CD terminal is repeatedly turning ON/OFF. Use the troubleshooting charts in Sections 11.3.5 and 11.3.6 to determine and correct the problem. Then repeat the loopback test.

(2) If data communications is not possible

The hardware settings or cable connections have probably not been done correctly.

Use the troubleshooting charts in Sections 11.3.2, 11.3.3, and 11.3.4 to determine and correct the problem and then repeat the loopback test.

(3) After the loopback test is finished, a computer link which uses the dedicated protocol is enabled.

When a computer link uses the no-protocol/bidirectional mode, do the following:

- Set the mode switches.
- Turn the power to the PC CPU OFF/ON or reset the PCCPU.

After doing the above, the computer link operation is enabled.

4.8 Inspection and Maintenance

The AJ71C24 module itself requires no particular inspection procedures. However, carry out the inspections listed in the PC CPU User's Manual to ensure optimum system performance.

5. HALF-DUPLEX COMMUNICATIONS USING THE RS-232C INTERFACE

This section explains how to do half-duplex communications using an RS-232C interface to connect an external device and an AJ71C24.

This section does not apply to full-duplex communications.

AJ71C24 can do half-duplex communications with an external device by using the RS-232C interface by setting buffer memory.

While receiving data from an external device in half-duplex communications, data is not transmitted from the AJ71C24 to the external device.

The key points for doing half-duplex communications between an external device and the AJ71C24 using the RS-232C connector are as follows:

- System configurations and functions
- Buffer memory settings
- Wiring
- ON/OFF timing of the CD and RS signals of the AJ71C24

5.1 System Configurations and Functions

The following figure shows (a) the system configurations of the external device and the PC CPU that can do half-duplex communications, and (b) the functions of the AJ71C24

Functions / System Configurations (external device : PC CPU)	Dedicated Protocol		No-protocol Mode/Bidirectional Mode
	Data Communications by a Command Transmitted from the External Device	Data Send from the PC CPU by the On-demand Function	Data Send and Data Receive
1 : 1	o	o*1	o*2
1 : n	o	x	x

o: Usable
x: Unusable

*1 During data communicates, the send timing of data that a sequence program requested to send changes due to the on-demand function.

See Section 8.14.2.

The send timing also changes as mentioned in *2 below.

*2 Send timing of data sent from the AJ71C24 and the external device changes according to the set timing of "priority/non-priority at the simultaneous transmission" set with the AJ71C24.

See Section 5.4.

5.2 Buffer Memory Settings

The following describes the buffer settings of the AJ71C24 for doing half-duplex communications.

Perform the following settings with the sequence program only when the AJ71C24 READY signal is turned ON after the CPU is reset or when the PC CPU is turned ON or (b) the higher byte in the mode switching designation area (address 119H) of the AJ71C24's buffer changes to 02H when the mode is switched.

Section 7.2 gives setting details.

(1) Communications setting using the RS-232C interface (Address 10FH)

Set "1" to do half-duplex communications.

(2) Setting of priority/non-priority at the simultaneous transmission (Address 110H)

When the AJ71C24 and the external device begin transmitting data simultaneously in half-duplex communications, designate (a) continuation (priority) of the send from the AJ71C24, or (b) interruption (non-priority).

Set "0" to designate " priority ".

Set "1" to "225" to designate " non-priority ".

This set value is the send wait time (unit :10 msec), until data transmission starts, after the data send state is restarted.

POINT

When an AJ71C24 is set to " priority ", the AJ71C24 keeps on transmitting data and ignoring received data. Even if data is transmitted from the external device after the AJ71C24 has started data transmission.

The external device that transmits data must execute the following so that the AJ71C24 does not ignore received data:

- Transmit response messages to start communications
- Resend data when a time out error of a response message occurs.

(3) Setting the method of resend (Address 111H)

When setting " half-duplex communications " + " non-priority " according to (1) and (2), this setting becomes valid.

As for simultaneous transmission from the external device and the AJ71C24, when the AJ71C24 restarts the send after interruption of the send, designate whether the interrupted message is transmitted again from the beginning ("resend") or only the remaining part is transmitted ("not resend").

Set "1" to designate " resend ".

Set "0" to designate " not resend ".

5.3 Wiring

The following describes the wiring for connecting the external device to the AJ71C24.

To do half-duplex communications, the CD signal of the AJ71C24 must be controlled by the external device.

Connect them according to "Connections to a device which can turn the CD terminal signal ON" shown in Section 4.5.2.

Section 5.4 describes the ON/OFF timing of the CD signal of the AJ71C24.

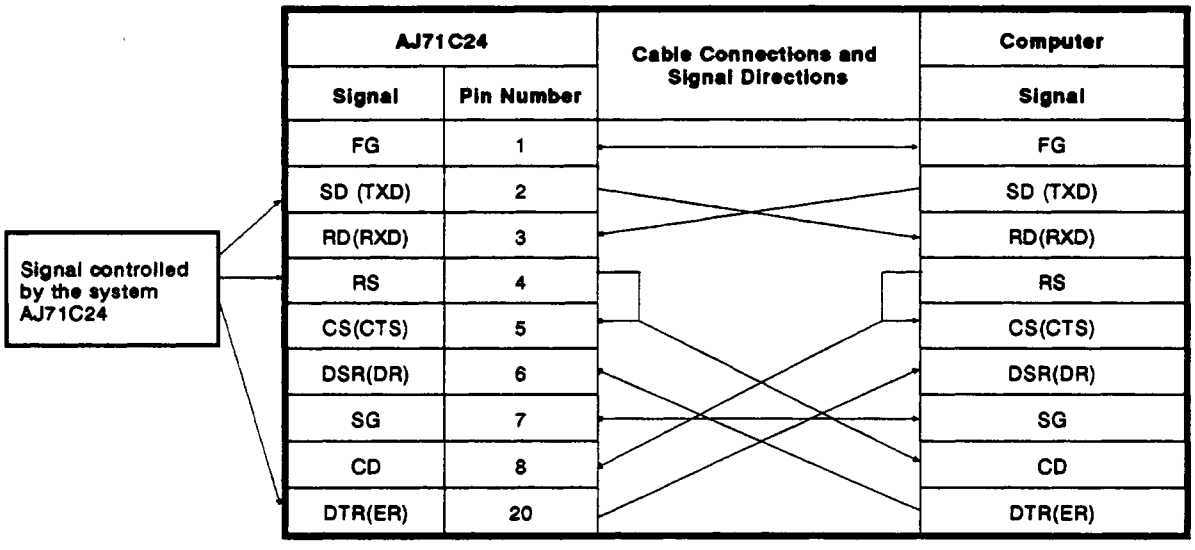
5.4 ON/OFF Timing of the CD and RS Signals of the AJ71C24

When doing half-duplex communications, the data transmission timing is shown by using the CD and RS signals of the AJ71C24.

In half-duplex communications, an external device controls the CD signal of the AJ71C24.

The AJ71C24 system controls the RS signal of the AJ71C24.

The table below shows the half-duplex communications connections discussed in this section.



AJ71C24		Cable Connections and Signal Directions	Computer
Signal	Pin Number		Signal
FG	1		FG
SD (TXD)	2		SD (TXD)
RD(RXD)	3		RD(RXD)
RS	4		RS
CS(CTS)	5		CS(CTS)
DSR(DR)	6		DSR(DR)
SG	7		SG
CD	8		CD
DTR(ER)	20		DTR(ER)

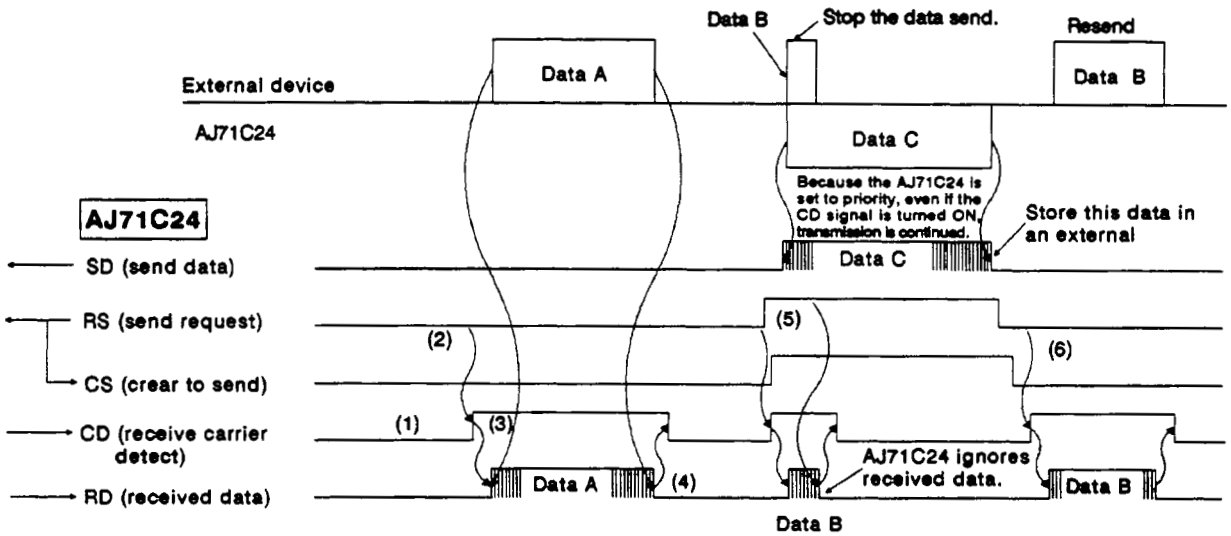
Example of Connections

5.4.1 Data transmission timing from an external device

When doing half-duplex communications, the data transmission timing from the external device is shown by using the CD and RS signals of the AJ71C24.

Setting the buffer memory of the AJ71C24 to "priority/non-priority at simultaneous transmission" controls the CD signal of the AJ71C24.

(1) AJ71C24 is set to " priority ".



The following steps describe the operations required for an external device at every timing mentioned by (1) to (6) in the above figure.

The signal names are of the signals of the AJ71C24.

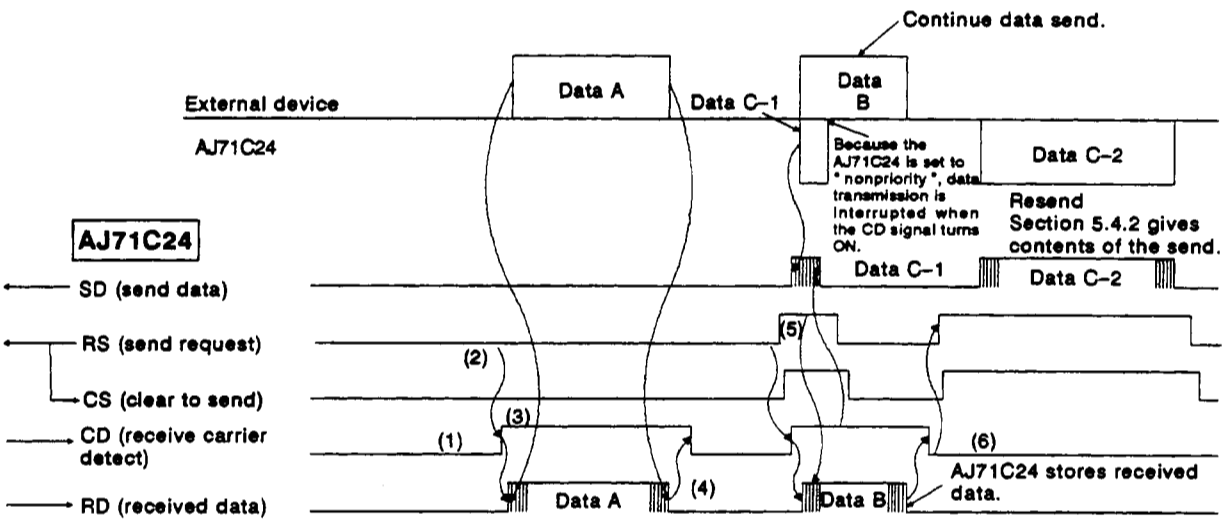
1) When not transmitting data from the external device to the AJ71C24, turn the CD signal OFF.
2) When doing a data send, check the RS signal. If the RS signal is OFF, turn the CD signal ON.
   If the RS signal is ON, wait until it turns OFF. After the RS is turned OFF, turn the CD signal ON.
3) After turning the CD signal ON, transmit data.
4) After completing the data send, turn OFF the CD signal .
5) If the RS signal turns ON during the data send, stop the data send. Then, turn the CD signal OFF, and perform data receive processing.
   (When the AJ71C24 and an external device start data transmission simultaneously, the RS signal turns ON.)
6) Retransmit all interrupted data from the external device to the AJ71C24 after the data send from the AJ71C24 is completed.

REMARK

When DTR/DSR control is being executed.

When (a) starting or during data transmission to the AJ71C24, (b) if the DTR(ER) signal of AJ71C24 turns OFF, interrupt data transmission until the DTR signal turns ON.
See Section 3.5.2.

(2) AJ71C24 is set to " non-priority ".



The following steps describe the operations required for an external device at every timing mentioned by (1) to (6) in the above figure.

The signal name is the signal of the AJ71C24.

As described in (1), turn ON/OFF the CD signal of the AJ71C24 with the external device and do data transmission to the AJ71C24.
(Note that 5) and 6) are different in the non-priority setting.)

1) When not transmitting data from the external device to the AJ71C24, turn the CD signal OFF.
2) When doing a data send, check the RS signal. If the RS signal is OFF, turn the CD signal ON.
   If the RS signal is ON, wait until it turns OFF. After the RS is turned OFF, turn the CD signal ON.
3) After turning the CD signal ON, transmit data.
4) After completing the data send, turn OFF the CD signal.
5) Even if the RS signal turns ON during data transmission, continue the data send to the AJ71C24. (This occurs when the AJ71C24 and the external device start data transmission simultaneously.)
6) After the send from the external device is completed, transmit data from the AJ71C24 to the external device.
   Section 5.4.2 gives details.

REMARK

When DTR/DSR control is being executed.

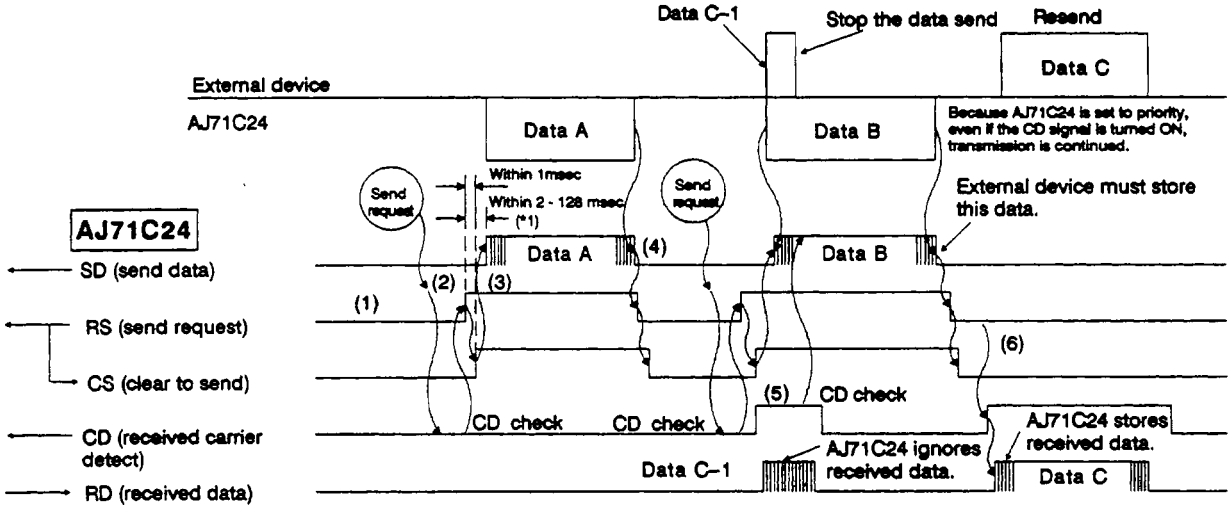
When (a) starting or during data transmission to the AJ71C24, and (b) if the DTR(ER) signal of AJ71C24 turns OFF, interrupt data transmission until the DTR signal turns ON.
See Section 3.5.2.

5.4.2 Data transmission timing from an AJ71C24

When doing half-duplex communications, data transmission timing from an AJ71C24 is shown by using the CD signal and RS signal of the AJ71C24.

Control the CD signal of the AJ71C24 by setting the buffer memory of the AJ71C24 to "priority/non-priority at simultaneous transmission" for data transmission.

(1) AJ71C24 is set to " priority ".



The following steps describe the operation at every timing mentioned by (1) to (6) in the above figure.

The signal names are of the signals of the AJ71C24.

As described in (1), turn ON/OFF the RS signal of the AJ71C24 with the external device and transmit data to the AJ71C24.

1) When not transmitting data from the external device to the AJ71C24, turn the RS signal OFF.
2) When doing a data send, check the CD signal. If the CD signal is OFF, turn the CD signal ON.
   When the CD signal is ON, wait until it turns OFF. After the CD is turned OFF, turn the RS signal ON.
3) After turning the RS signal ON, transmit data.
4) After completing the data send, turn OFF the RS signal.
5) If the CD signal turns ON during the data send, continue transmitting data send to the AJ71C24. (This occurs when the AJ71C24 and the external device start data transmission simultaneously.)
6) Transmit all interrupted data from the external device to the AJ71C24 after data send from the AJ71C24 is completed.

*1 The time from when the RS signal turns ON until communications start varies with the data transmission speed.
The faster the transmission speed is, the sooner communications will start.

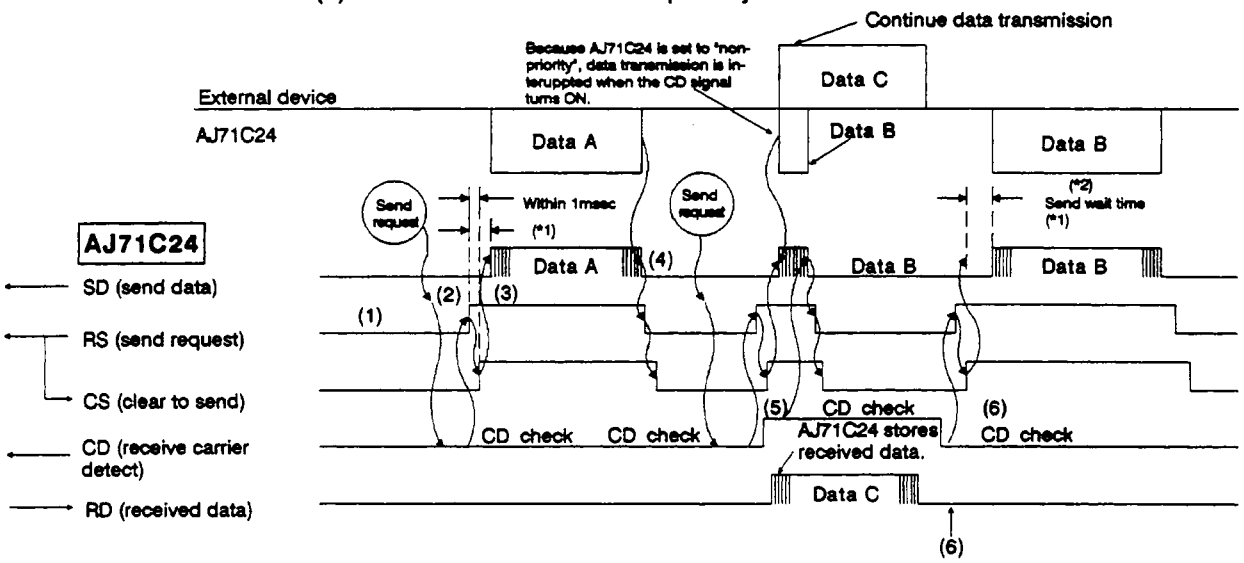
REMARK

When DTR/DSR control is being executed.

When (a) starting or during the data transmission to the AJ71C24, and (b) if the DSR(DR) signal of AJ71C24 turns OFF, interrupt data transmission until the DSR signal turns ON.

See section 3.5.2.

(2) AJ71C24 is set to " non-priority ".



The following steps describe the operations performed by AJ71C24 at every thing. The signal names are of the signals of the AJ71C24.

As described in (1), turn ON/OFF the RS signal of the AJ71C24 and do data transmission to the external device.

Note that 5) is different.

1) When not transmitting data from the external device to the AJ71C24, turn the RS signal OFF.
2) When doing a data send, check the CD signal. If the CD signal is OFF, turn the RS signal ON.
   If the CD signal is ON, wait until it turns OFF. After the CD is turned OFF, turn ON the RS signal.
3) After turning the RS signal ON, transmit data.
4) After completing the data send, turn OFF the RS signal.
5) If the CD signal turns ON during data send, stop the data send. Then, turn the RS signal OFF and perform data receive processing. (This occurs when the AJ71C24 and an external device start data transmission simultaneously.)
6) After transmission from the external device is completed, resend all data from the beginning, or transmit data remaining after the send interruption in 5).

*1 Data set at buffer address 110H is not transmitted.

*2 Resend all data from the beginning, or transmit data remaining after the send interruption according to the setting of buffer address 111H.

REMARK

When DTR/DSR control is being executed.

When (a) starting or during the data transmission to the external device and (b) if the DSR(DR) signal of AJ71C24 turns OFF, interrupt data transmission until the DSR signal turns ON.
See section 3.5.2.

6. DATA COMMUNICATIONS USING AN M : N MULTIDROP LINK

This section describes how to do data communications using an m : n multidrop link. This section only applies to m : n multilink data communications.

An AJ71C24 can perform data communications with several external devices by constructing a multidrop link consisting of several external devices (m stations) and several AJ71C24s (n stations). (The maximum number of m and n stations is 32.)

A computer link can be made with the full-duplex communications method using the RS-232C and RS-422 lines by constructing an m : n multidrop link. In addition, data transmission is initiated by a command from the external device in the dedicated protocol.

The key points for constructing an m : n multidrop link system involve:

- Methods of data communications
- Conditions and methods for interlocking external devices (computers)

6.1 Key Points

(1) When using an m : n multidrop link system, only one computer can perform data communications with a single PC CPU.

Set up the computers so that a computer and a PC CPU can do 1 : 1 communications. Sections 6.2 and 6.3 give the conditions and procedures for computer interlocking.

(2) Data communications between a computer and a PC CPU can only be done in the following way:

- Full-duplex communications must be used. (m : n data communications cannot be done with half-duplex communications.)
  Transmit a command from a computer using the dedicated protocol (except for protocol 3). Data communications with protocol 3 and data transmission from the sequence program using the on-demand function cannot be done.

(3) All computers (including the computer that transmitted the data) receive data from either computer. In addition, all computers receive data transmitted from a PC CPU. Therefore, every computer that receives data addressed to other stations (as specified by the station number in the message) must ignore that data.

The AJ71C24 which is connected to the PC CPU ignores the receive data which is addressed to other stations.

(4) The station number of a computer is expressed as eight-bit data. Use switch SW12 to set the data bit for communications to eight bits (see Section 6.2.1).

Section 4.3.2 gives details about switch SW12.

6.2 Conditions for Computer Interlock

When constructing an m : n multidrop link using computers and PC CPUs, all computers must be interlocked to prevent several computers from simultaneously communicating with PC CPUs.

This section explains how to interlock computers to allow data communications between a computer and a PC CPU. The term "interlocking" used in this section means the procedure which provides a computer priority to use a communications line. This priority is called an "access right".

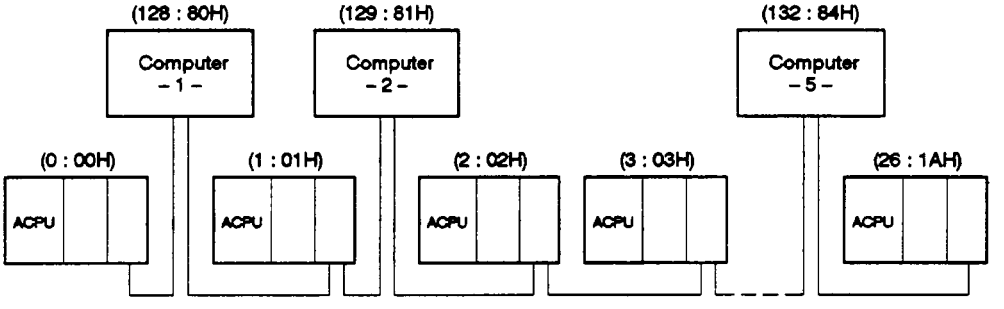
6.2.1 Computer station number allocation

For data communications with a designated computer, allocate a station number within the range of 128 to 159 (80H to 9FH) to each computer.

Set the station number for broadcasting to all computers at 160 (AOH).

Example: m : n = 5 : 27

( ) shows each station number of a computer and an AJ71C24.
(Decimal: hexadecimal)

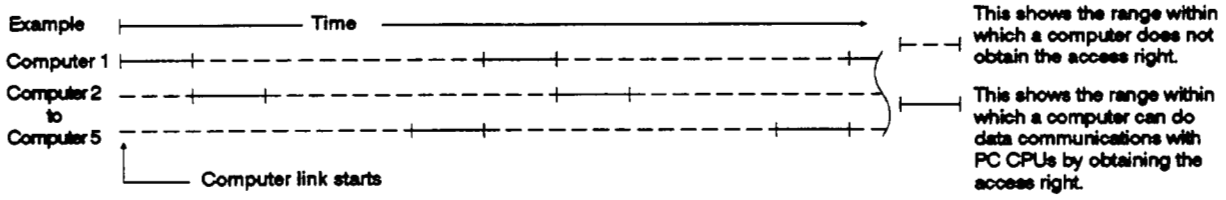


6.2.2 Maximum data communications time per computer

Set the maximum time so that, after obtaining an access right, each computer can perform data communications with PC CPUs.

(In the following figure, each of these ⊢——⊣ means time duration.)

Even if the computer that obtains the access right malfunctions, data communications can be done between other computers and PC CPUs by setting the maximum data communications time.


Example
Time
Computer 1
Computer 2
to
Computer 5
Computer link starts
This shows the range within which a computer does not obtain the access right.
This shows the range within which a computer can do data communications with PC CPUs by obtaining the access right.

POINT

Set the maximum data communications time per computer to a time that is sufficient for data communications with PC CPUs in the computer link system.

After the computer link system starts, the computer that obtains the access right must complete data communications with PC CPUs within the maximum data communications time.

(When unable to complete data communications, the computer with the access right transmits the CL code to communicating PC CPUs within the maximum data communications time, and initializes a transmission sequence to an AJ71C24.)

While a computer and PC CPUs are performing data communications, the time-out check function must be used with other computers to block data transmission from those computers.

6.2.3 Command and message format for data communications among computers

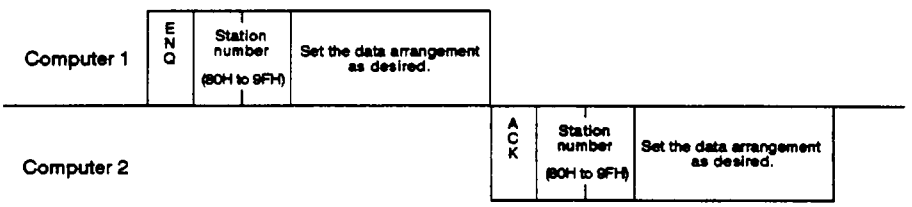
A command and message format for data communications among computers with the dedicated protocol must be set.

Use any command except the commands used with the dedicated protocol of an AJ71C24. See Section 3.3.1.

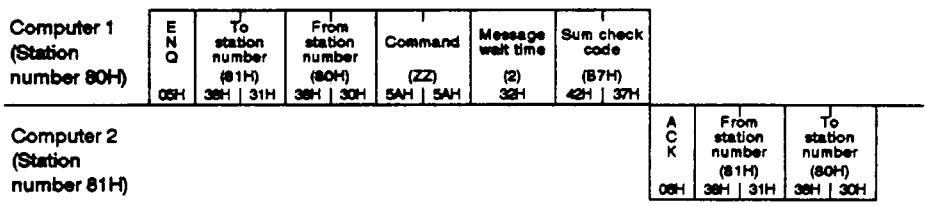
The message format basically follows the control procedure set by the mode setting switch of each AJ71C24. See Section 8.4.

Set the data arrangement after the PC number in the message as desired.

(1) Protocol 1 when doing data communications



(2) Example of a message format (when station numbers 80H and 81H perform data communications)


Computer 1 (Station number 80H)
ENQ 05H
To station number (81H) 38H 31H
From station number (80H) 38H 30H
Command (ZZ) 5AH 5AH
Message wait time (2) 32H
Sum check code (B7H) 42H 37H
Computer 2 (Station number 81H)
ACK 06H
From station number (81H) 38H 31H
To station number (80H) 38H 30H

REMARK

(1) If the mode setting switch of an AJ71C24 is set for the dedicated protocol mode (1 to 4) and if the station number written in a message to be transmitted from computer 1 is 00H to 31H (designating AJ71C24), then the designated station (AJ71C24) determines that message to be a faulty message and it transmits back a message beginning with NAK to computer 1. Always use station numbers 80H to 9FH for communications between the computers.

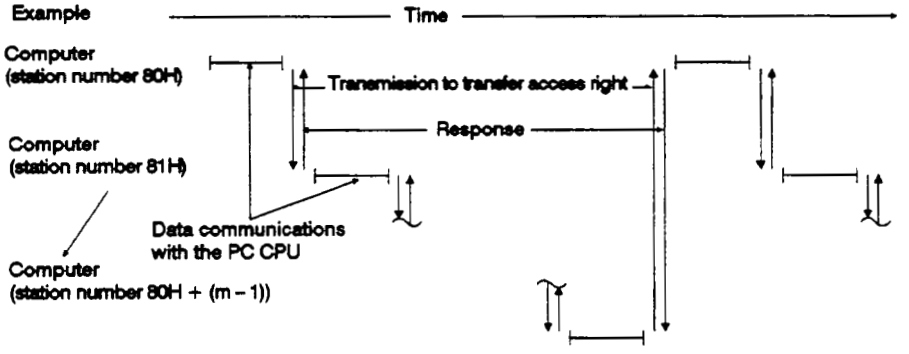
(2) Section 8.3 tells how to read the message format figures.

6.3 Procedure for Data Communications with a PC CPU

This section explains the procedure for computer interlocking and data communications with a PC CPU when constructing an m : n multidrop link.

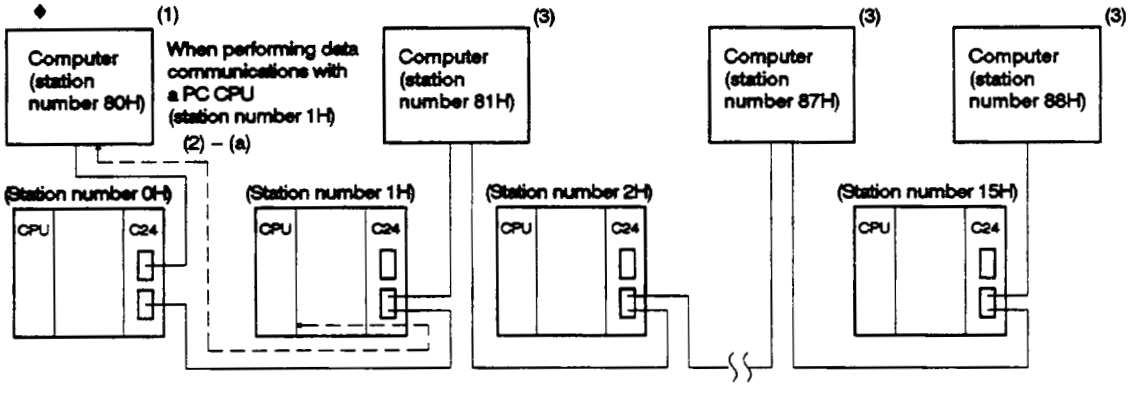
6.3.1 Communications between each computer and PC CPUs

Each computer obtains the access right (one after another according to the order of the station number of each computer) and then does data communications with PC CPUs.



The following example shows the procedure for data communications between each computer and PC CPUs.

◆: Computer with the access right



(1) When starting a system, the computer allocated with the minimum station number (80H) obtains the access right.

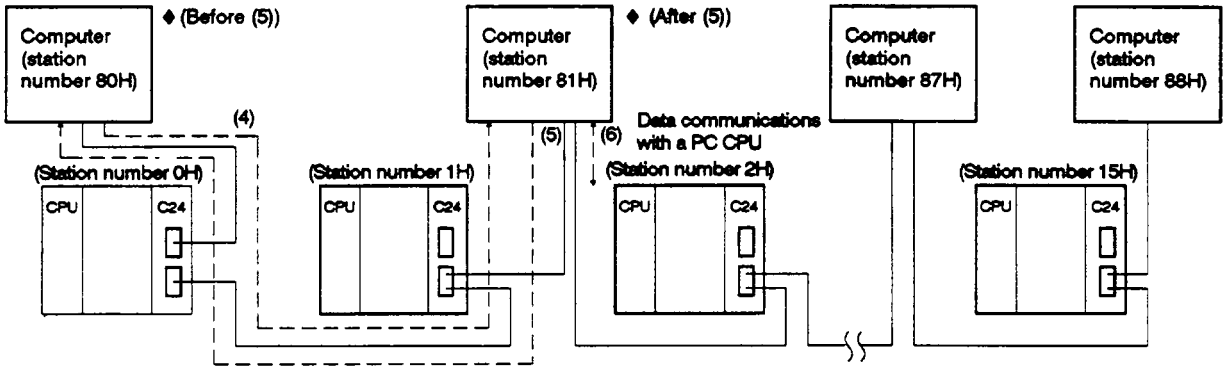
(2) The computer which has the access right:

(a) Performs data communications with PC CPUs within the maximum data communications time set among computers, and then, starts procedure (4).

(b) Starts procedure (4) if it does not perform data communications with PC CPUs.

(3) Each computer without the access right checks the access right time (the maximum data communications time) of the computer with the access right and ignores incoming data which is addressed to others. When the access right time exceeds the maximum data communications time, each computer executes the processing mentioned in (7).

●: Computer with the access right

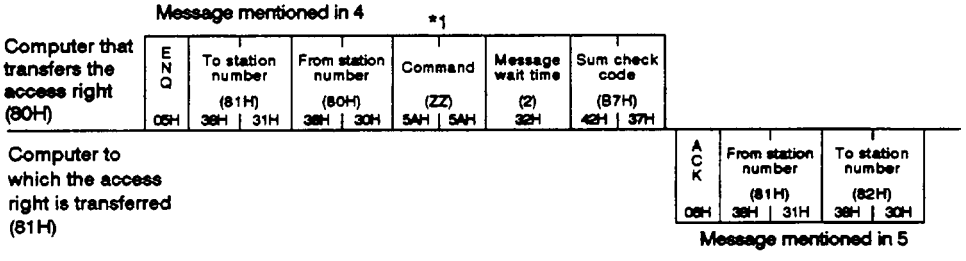


(4) The computer that has finished data communications with PC CPUs and the computers that do not need data communications with PC CPUs transmit the access right transfer data to the computer at the next station number.

When a computer is unable to receive a response message from the next computer to which the access right is to be transferred, it keeps on transmitting the access right transfer data to the following computers in the order of station numbers until the access right transfer is completed.

(5) The computer to which the access right is given transmits a response message to the computer that gave the access right.

(An example of data communications using dedicated protocol 1)



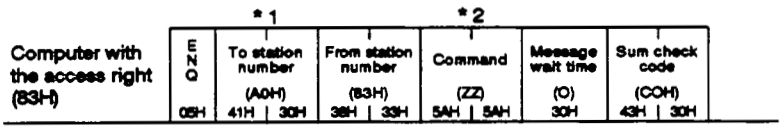
*1 The command symbol "ZZ" in this example is indicated only for explanation. Use any desired symbol for the transfer command to obtain the access right. See Section 8.3 tells how to read the message format figure.

(6) The computer that transmitted a response message and obtained the access right executes the processing mentioned in (2).

(7) When the access right time of a computer with the access right exceeds the maximum data communications time

(a) The computer at the next station number transmits broadcast data to all computers, obtains the access right, and executes the processing mentioned in (2).

(An example of data communications using dedicated protocol 1)



(b) Other computers check if they received the data transmitted to all computers.

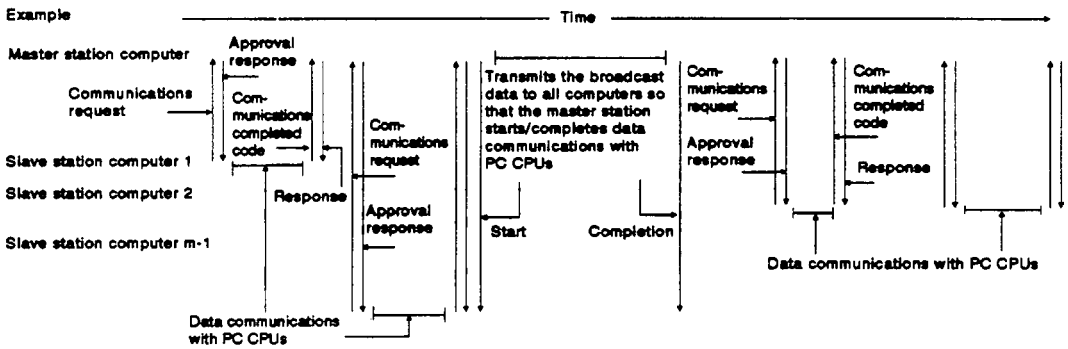
Computers which received the data execute the processing mentioned in (3).

If a computer failed to receive the data, the next computer transmits data to all computers, obtains the access right, and executes the processing mentioned in (2).

Other computers execute the check mentioned above.

6.3.2 Data communications with PC CPUs by setting a master station and slave stations

One of the computers is set as a master station and the other computers are set as slave stations which need the approval of the master station to perform data communications with PC CPUs.



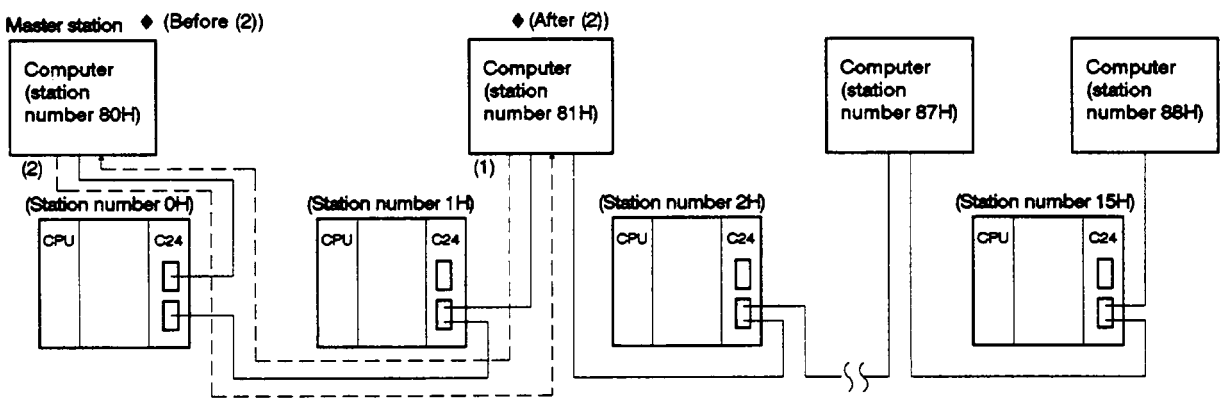
The following example shows how each computer performs data communications with PC CPUs.

After the start of data communications between a computer and PC CPUs, each computer executes the time-out check of the maximum data communications time.

A computer at a slave station that is not performing data communications with a PC CPU checks the communications completed code which is transmitted from the computer when it has completed data communications with PC CPUs.

In the following figure, the computer at the minimum station number 80H is set as the master station and other computers are set as slave stations.

♦ : Computers with the access right

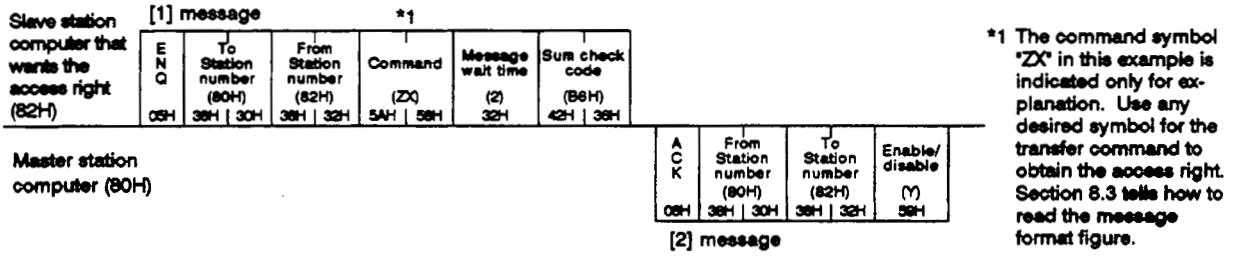


(1) A slave station that requires data communications with a PC CPU transmits a communications request to obtain the access right to the master station.

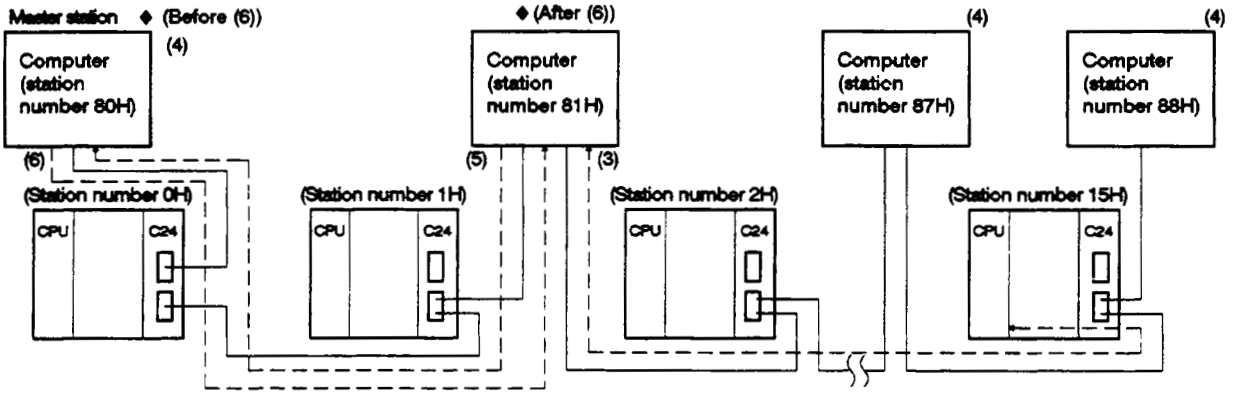
An example of the message format is shown in (2) below.

(2) The master station transmits an approval response to the slave station that made the communications request.

(An example of data communications using dedicated protocol 1)


Slave station computer that wants the access right (82H)
[1] message
*1
ENQ 05H
To Station number (80H) 38H 30H
From Station number (82H) 38H 32H
Command (ZX) 5AH 58H
Message wait time (2) 32H
Sum check code (B6H) 42H 36H
Master station computer (80H)
ACK 06H
From Station number (80H) 38H 30H
To Station number (82H) 38H 32H
Enable/ disable (Y) 59H
[2] message
*1 The command symbol "ZX" in this example is indicated only for explanation. Use any desired symbol for the transfer command to obtain the access right. Section 8.3 tells how to read the message format figure.

♦ : Computer with the access right



(3) After performing data communications with a PC CPU within the maximum data communications time set among computers, the slave station that received an approval response executes the processing as shown in (5) below.

(4) The master station that transmitted the approval response and the slave stations that do not have the access right check the access right time of the slave station that obtains the access right, and, ignore received data which is addressed to other stations.

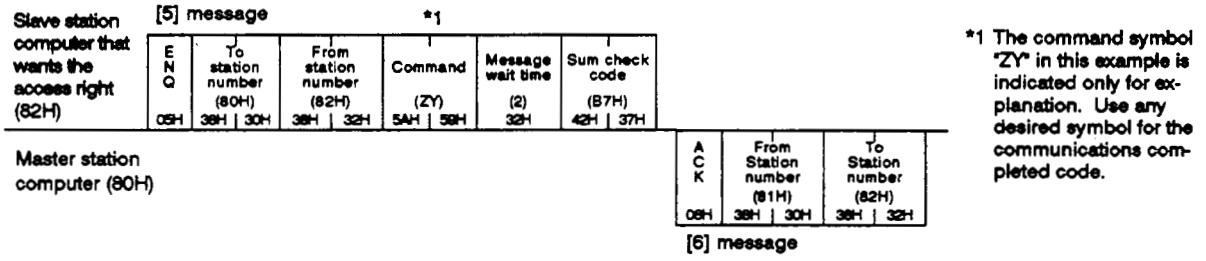
If the access right time of a computer with the access right exceeds the maximum data communications time, each computer executes the processing mentioned in (7).

(5) A slave station that has finished data communications with PC CPUs transmits the communications completed code to the master station. An example of the message format is shown in (6) below.

Slave stations which are not performing data communications with PC CPUs check the transmission of the communications completed code. During this checking, the slave stations must not perform data communications with the master station.

(6) The master station that received the communications completed code transmits a response to the slave station that transmitted the communications completed code.

(An example of data communications using dedicated protocol 1)


Slave station computer that wants the access right (82H)
[5] message
*1
ENQ 05H
To station number (80H) 38H | 30H
From station number (82H) 38H | 32H
Command (ZY) 5AH | 59H
Message wait time (2) 32H
Sum check code (B7H) 42H | 37H
Master station computer (80H)
ACK 06H
From Station number (81H) 38H | 30H
To Station number (82H) 38H | 32H
[6] message
*1 The command symbol "ZY" in this example is indicated only for explanation. Use any desired symbol for the communications completed code.

(7) After the processing given in (6) is completed or when the access right time of a slave station with the access right exceeds the maximum data communications time:

(a) The master station waits for a communications request from a slave station.

When the master station receives a communications request, the processing mentioned in (2) is executed.

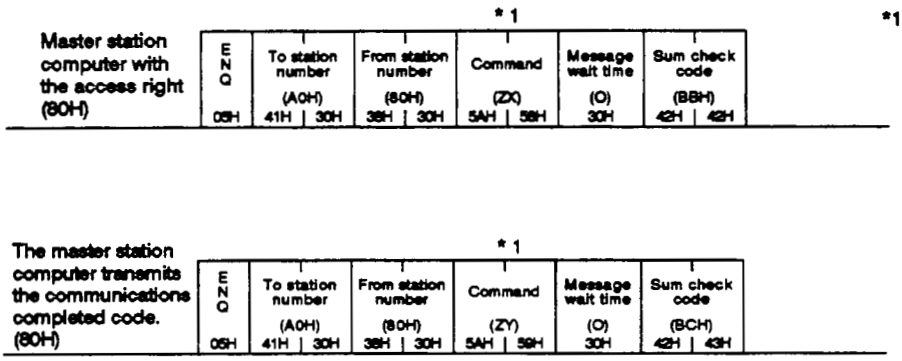
(b) Until data communications with PC CPUs is required, a slave station does not perform data communications with the master station.

When data communications with PC CPUs is required, the processings in and after (1) are executed.

(8) If no slave station obtains the access right, the master station transmits broadcast data to all stations and obtains the access right and performs data communications with PC CPUs.

The master station transmits the broadcast data to all computers after completing data communications with PC CPUs to inform slave stations of the completion of data communications with PC CPUs.

(An example of data communications using dedicated protocol 1)



*1 The command symbols "ZX" and "ZY" in this example are indicated only for explanation. Use any desired symbol for communications between the master station and slave stations.

7. INITIAL SETTING OF TRANSMISSION CONTROL DATA TO BUFFER MEMORY

The buffer memory has a special applications area for setting transmission control data for communications with external devices (see Section 3.7).

Each transmission data item has a default value. However (depending on the purpose and application of data transmission), using default values not only makes data communications more complicated, but may even preclude them. This section describes the settings of all items in the buffer memory special applications area, shows how to make changes, and gives specific examples.

The following sections give detailed information about the special applications area:

- Section 8.14 gives details about the special applications area used for the on-demand function when dedicated protocols are used.
- Section 9.5 (5) gives details about the no-protocol received data clear request area when the no-protocol mode is used.
- Section 10 gives details about the special applications area when the bidirectional mode is used.

POINTS

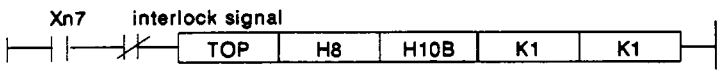
(1) This section also discusses changing the default values set in the special-applications area in the buffer and reading the present values of the special-applications area.

It is not necessary to write setting values to an area where default values do not have to be changed.

(2) When changing a setting (except for the two areas indicated below), either (a) turn ON the power supply or reset the PC CPU and change the setting after the AJ71C24 READY signal (Xn7) goes ON, or (b) switch the AJ71C24 mode and change the setting after the higher bytes in the designated mode switching area of the AJ71C24 buffer are moved into 02H.

- Error LED turn-OFF request area (address 102H)
- Mode switching designation area (address 119H)

Example: How to disable the RS-232C CD terminal check function



(3) Buffer memory addresses 10E and 11DH to 11FH are reserved for the system only. Writing data to these addresses precludes normal operation of the AJ71C24.

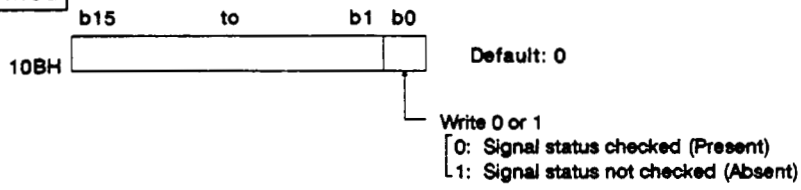
7.1 Setting RS-232C CD Terminal Check Enable/Disable

Setting this RS-232C CD terminal check function to enable or disable determines whether or not the AJ71C24 checks the ON/OFF status of the CD signal (receive carrier detection signal).

Disabling the RS-232C CD terminal check function.

If a "1" is written to buffer memory address 10BH, the AJ71C24 does not check the ON/OFF status of the CD signal. It operates as if the CD signal were ON.

Setting Method



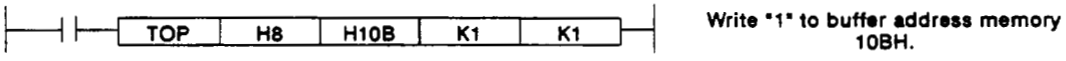
POINT

Set bits b1 to b15 of address 10BH to either 0 or 1.
(The AJ71C24 will ignore the settings.)

Example

How to disable the RS-232C CD terminal check function (AJ71C24 I/O addresses 80 to 9F).

(Sequence Program)



POINT

When the RS-232C is set to use half-duplex transmission (see Section 7.2), set the CD terminal check to "Enabled". Section 4.5.2 explains the connecting procedure.

If the CD terminal check is set to "Disabled", the transmission method is automatically set to full-duplex transmission.

7.2 Setting the Transmission Method for RS-232C

Set the transmission method used with the RS-232C interface which connects the AJ71C24 to the external device. Both half-duplex and full-duplex transmissions can be used for setting. If the half-duplex transmission is used, the following settings should be made:

- Whether or not the AJ71C24 continues or stops transmission when the AJ71C24 and the external device have begun sending data to each other at the same time. (Priority/non-priority setting at simultaneous transmission)
- Whether or not the AJ71C24 transmits data again from the beginning or from the point where transmission stopped when it restarts transmission. (Transmission method when the transmission restarts.)

Set the transmission method which conforms to the specifications of the connected device.

POINT

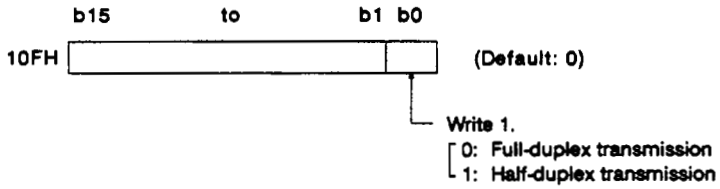
- When full-duplex transmission is used, settings with buffer memory addresses 10FH, 110H, and 111H are not required.
- Section 5.2 gives settings required for half-duplex transmission.
- When using half-duplex transmission, set the RS-232C CD terminal check to "Enabled" (see Section 7.1).

7.2.1 Setting priority of transmission to the AJ71C24 using half-duplex transmission

The following shows how to set the AJ71C24 to continue transmission when the AJ71C24 and an external device (using half-duplex transmission) have begun sending data to each other simultaneously.

Setting Method

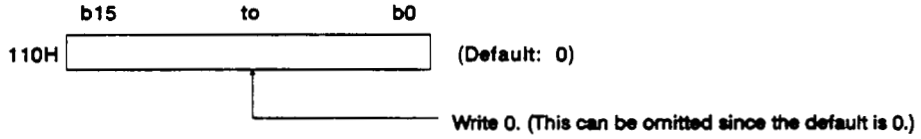
(1) Transmission method



POINT

- Set bits b1 to b15 of address 10FH to either 0 or 1. (The AJ71C24 will ignore the settings.)

(2) Priority setting when transmission has begun at the same time



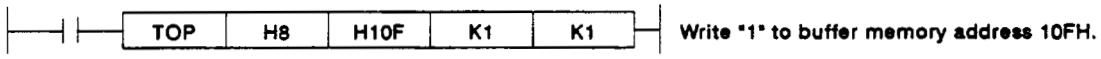
POINT

If the priority of transmission is set, setting to buffer memory address 111H is not required.

Example

The CD terminal check is set to "Enabled". Half-duplex transmission is used and the priority of transmission is set. (AJ71C24 I/O addresses: 80 to 9F)

(Sequence Program)



Write "1" to buffer memory address 10FH.

Leave the setting of buffer memory addresses 10BH and 110H for defaults.

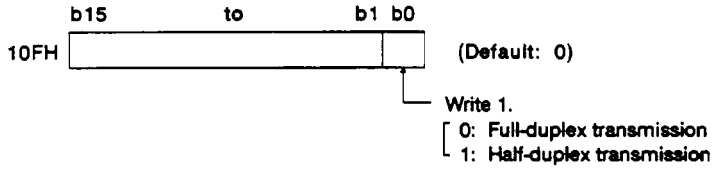
7.2.2 Setting non-priority of transmission to the AJ71C24 with the half-duplex transmission

The following shows how to set the AJ71C24 to discontinue transmission when the AJ71C24 and an external device (using half-duplex transmission) have begun transmitting data to each other simultaneously.

(1) Setting "half-duplex transmission", "non-priority", and "not resend":

Procedure

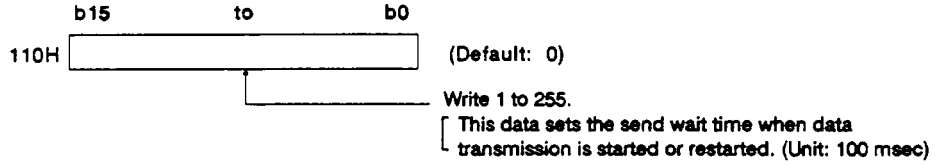
(1) Transmission method



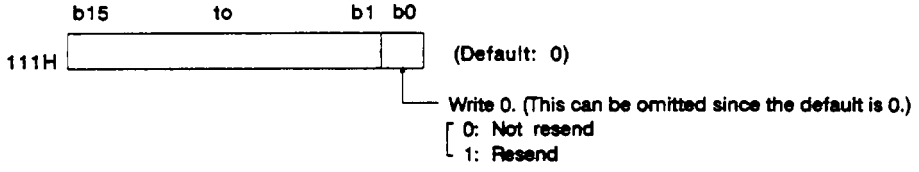
POINT

- Set bits b1 to b15 of address 10FH to either 0 or 1. (The AJ71C24 will ignore the settings.)

(2) Priority setting when transmission has begun simultaneously



(3) Transmission method when data transmission is restarted



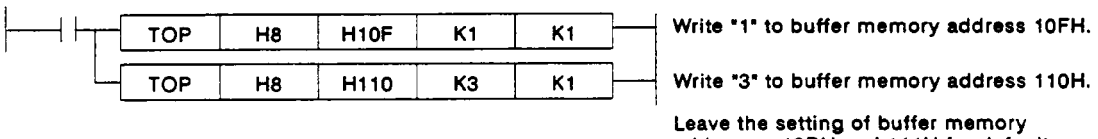
POINT

Set bits b1 to b15 of address 111H either to 0 or 1. (The AJ71C24 will ignore the settings.)

Example

The CD terminal check is set to "Enabled". Half-duplex transmission is used and the non-priority of transmission and "not resend" are set. (Send wait time: 300 msec) (AJ71C24 I/O addresses: 80 to 9F)

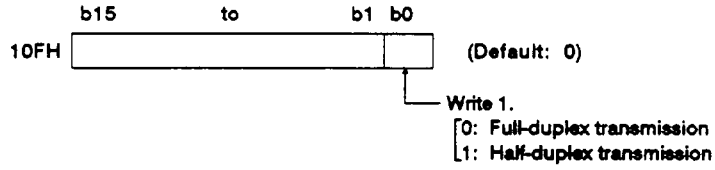
(Sequence Program)



(2) To set "half-duplex transmission", "non-priority", and resend.

Setting Method

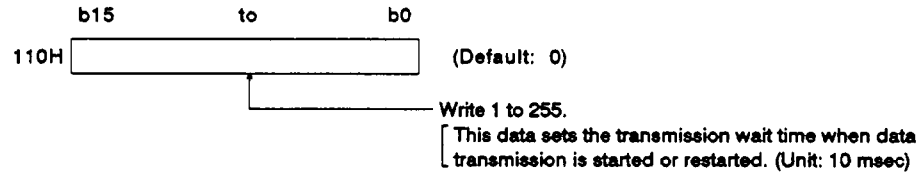
(1) Transmission method



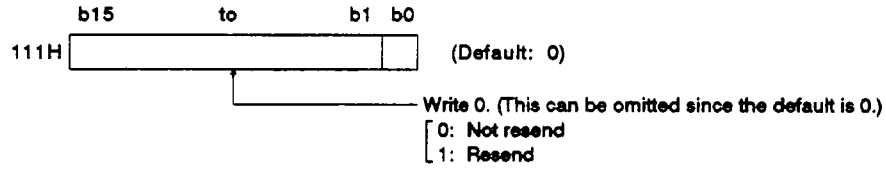
POINT

Set bits b1 to b15 of address 10FH to either 0 or 1. (The AJ71C24 will ignore the settings.)

(2) Priority setting when transmission has begun simultaneously



(3) Transmission method when data transmission is restarted



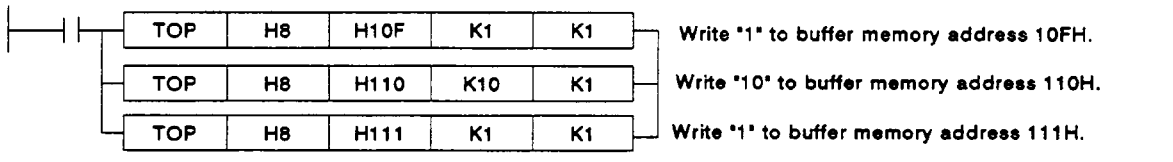
POINT

Set bits b1 to b15 of address 111H to either 0 or 1. (The AJ71C24 will ignore the settings.)

Example

The CD terminal check is set to "Enabled". Half-duplex transmission is used and the non-priority of transmission and "resend" are set. (Send wait time: 100 msec) (AJ71C24 I/O addresses: 80 to 9F)

(Sequence Program)


TOP H8 H10F K1 K1
Write "1" to buffer memory address 10FH.
TOP H8 H110 K10 K1
Write "10" to buffer memory address 110H.
TOP H8 H111 K1 K1
Write "1" to buffer memory address 111H.

Leave the setting of buffer memory address 10BH for default.

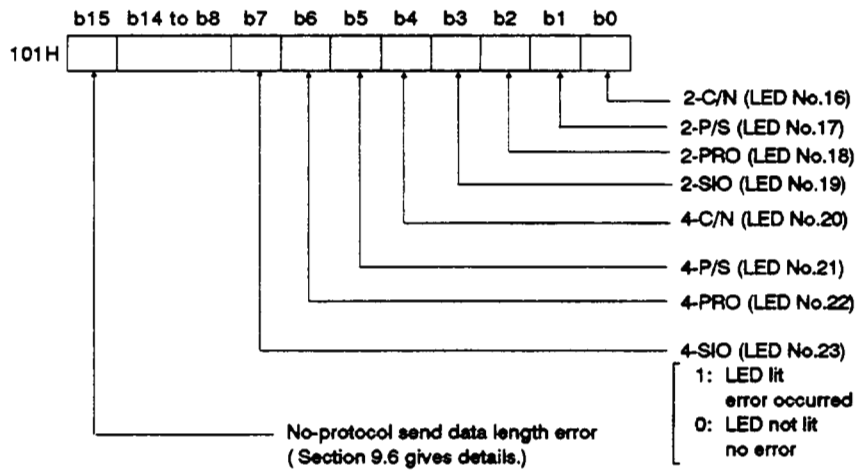
7.3 Reading Transmission Error Data

This section explains the contents of the buffer memory area where the ON/OFF status of the error LEDs are stored. It also shows how to turn LEDS which are lit OFF.

7.3.1 Reading the error LED display status

(1) Error LED display status storage area

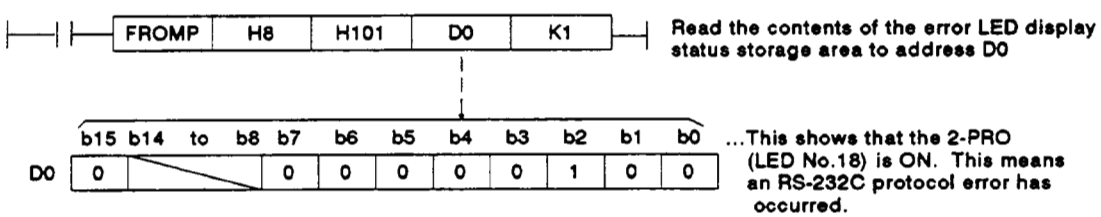
The ON/OFF status of the error LEDs are stored in address 101H of the buffer memory (see below).



(2) Program example to read the error LED display status storage area

This gives an example of a program using the sequence program [FROM] to read the error LED display ON/OFF status stored in buffer memory address 101H.

Program example to read the error LED display status storage area (AJ71C24 I/O addresses 80 to 9F)


FROMP
H8
H101
D0
K1
Read the contents of the error LED display status storage area to address D0
b15 b14 to b8 b7 b6 b5 b4 b3 b2 b1 b0
D0
0 0 0 0 0 0 0 1 0 0
...This shows that the 2-PRO (LED No.18) is ON. This means an RS-232C protocol error has occurred.

REMARK

Section 4.2.2 gives details about the ON/OFF state of each bit in the error LED display area.

Section 11 gives details about error processing.

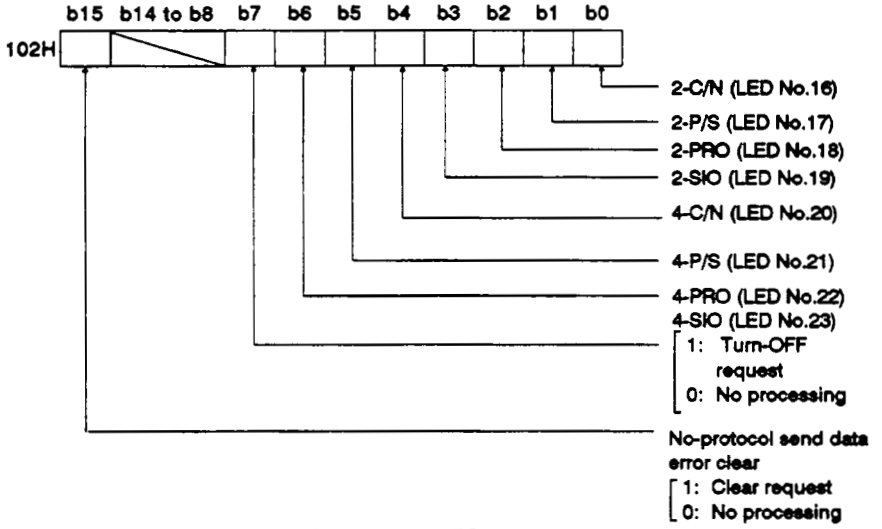
Sections 3.5.2 and 3.5.3 give details about 2-SIO (LED No.19) and 4-SIO (LED No.23).

7.3.2 Turning OFF error LEDs

When an error LED turns ON, it stays ON (lit) even when the cause of the error has been eliminated.

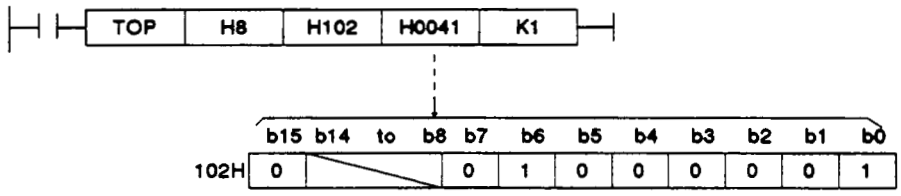
To turn OFF the lit LED, "1" must be written to the appropriate bit of address 102H of the buffer memory, using the sequence program TO instruction.

(1) Error LED turn-OFF request area



(2) Program example to turn OFF error LEDs

A sequence program example to turn OFF LED 2-C/N (LED No.16) and LED 4-PRO (LED No.22) is given below.



POINTS

(1) The LED turn-OFF request is only valid when it is written.

(2) Relevant data in the error LED display status storage area at address 101H is cleared when the LED turn-OFF request is made. Data at address 102H remains as written.

(3) If the error data has not been cleared after the LED turn-OFF request is made, the corresponding bit in the error LED display status storage area turns the error LED ON again.

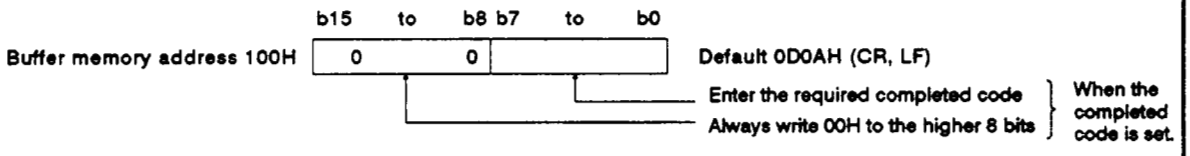
7.4 Settings in the No-Protocol Mode

This section describes setting methods and gives no-protocol mode examples.

7.4.1 Setting the no-protocol mode receive-completed code (for receive with variable-length data)

How to set and modify the receive-completed code and the sequence program for the receive processing with variable-length data are shown below.

Setting Method


b15 to b8 b7 to b0
Buffer memory address 100H
0
0
Default 0D0AH (CR, LF)
Enter the required completed code
Always write 00H to the higher 8 bits
When the completed code is set.

POINTS

(1) The completed code can be set to any value which makes 1 byte in the range of 00H to FFH. Since the default value setting is 0D0AH, when the CR and LF codes are received during the data receive, the read request is transmitted to the sequence program (Xn1 is ON). If the default setting has been changed, when a modified completed code is received during the data receive, the read request is transmitted to the sequence program.

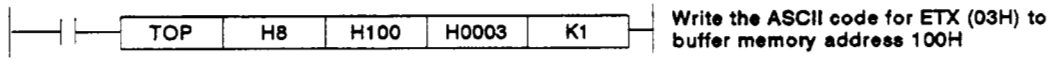
(2) If the length of data to complete data receive is also set, the read request for the received data is transmitted when the completed code or the set length of data (whichever comes first) is received. (Xn1 is ON)

(3) If the completed code is not set, set buffer memory address 100H to FFFFH. This enables only the setting of data length to complete receive, and the read of received data by fixed data length is enabled.

Example

To set the end code to ETX (03H) (AJ71C24 I/O addresses 80 to 9F)

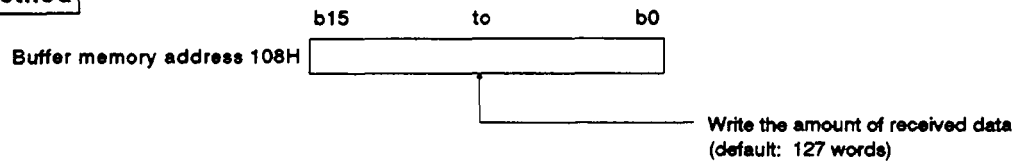
(Sequence Program)



7.4.2 Specifying no-protocol receive completion data length (fixed length)

How to complete the data receive and set the data length are given below along with a sequence program example.

Setting Method



POINTS

(1) Set the length of data to complete the data receive in the following ranges:

Length of data received ≤ no-protocol mode buffer size (when word units are set)

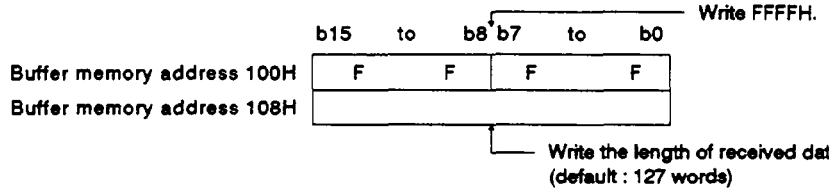
Length of data received ≤ no-protocol mode buffer size x 2 (when byte units are set)

If the received data length is larger than the no-protocol mode buffer size, then it is automatically set equal to the no-protocol mode buffer size.

(2) Section 7.4.3 describes the selection of a word or byte unit for the data length to complete data receive.

(3) If the receive-completed code is set, the read request for the received data is transmitted when the completed code or the set data length (whichever comes first) is received. (Xn1 is ON)

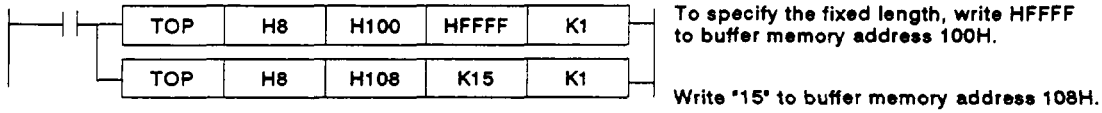
(4) To read the received data by fixed length without setting the completed code, do the following setting:



Example

To set the fixed length at which data receive is complete to 15 words in the case of the read of received data only by fixed length (AJ71C24 I/O addresses 80 to 9F)

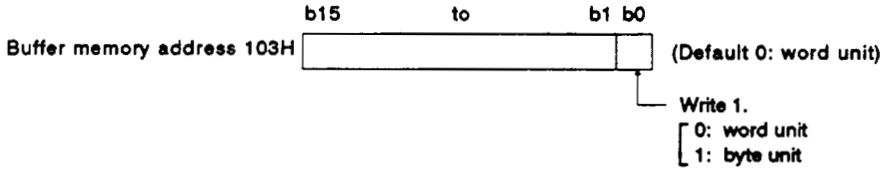
(Sequence Program)



7.4.3 Setting a word or byte unit in the no-protocol mode

This section shows how to set the word or byte unit for data communications and gives an example.

Setting Method



POINTS

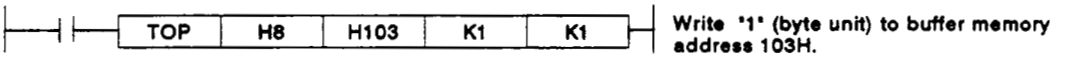
(1) The word or byte unit set here only applies to comunications data in the no-protocol/bidirectional mode and on-demand data using a dedicated protocol.

(2) Set bits b1 to b15 of address 103H to either 0 or 1. (The AJ71C24 will ignore the settings.)

Example

To set the byte unit (AJ71C24 I/O addresses 80 to 9F)

(Sequence Program)

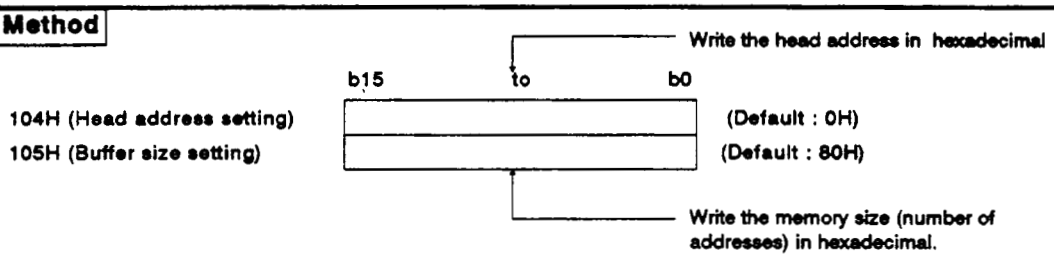


7.4.4 Setting a buffer memory area for no-protocol send

This section describes how to set the AJ71C24 buffer memory area to store data transmitted from the PC CPU to an external device in the no-protocol mode and gives an example.

When the bidirectional mode setting area (address 112H) is set to "1", this memory area is set for bidirectional mode transmission.

Setting Method



POINTS

(1) Buffer memory addresses 100H to 11FH are for the special applications area and should not be set.

(2) When other kinds of devices are also used, make sure that the specified range does not overlap the no-protocol receive area or the on-demand data area.

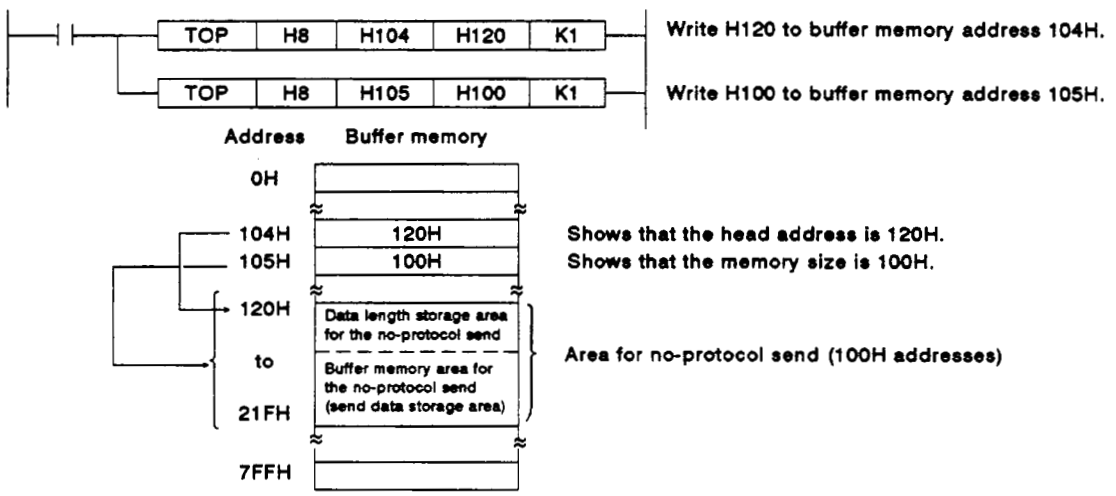
(3) Buffer memory address 105H should include the storage area of the no-protocol send data length.

(4) If any range except the user area is set, the AJ71C24 will execute operations with defaults including the areas mentioned in (2) above.

Example

To set the head address to 120H and the memory size to 100H (AJ71C24 I/O addresses 80 to 9F).

(Sequence Program)

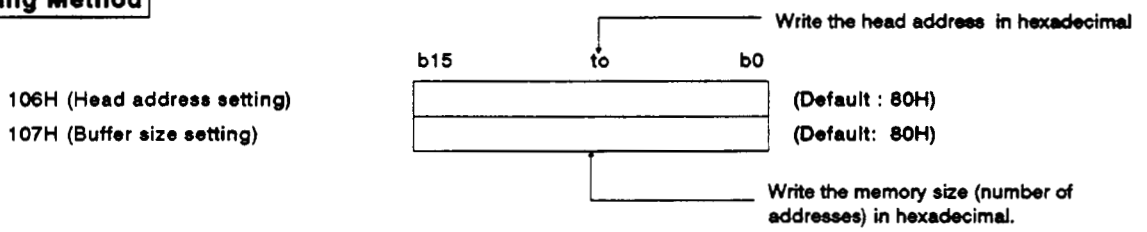


7.4.5 Setting a buffer memory area for no-protocol receive

This section shows how to set the AJ71C24 buffer memory area to store data the PC CPU received from the external device in the no-protocol mode. An example is also given.

When the bidirectional mode setting area (address 112H) is set to "1", this memory area is set for bidirectional mode transmission.

Setting Method



POINTS

(1) Buffer memory addresses 100H to 11FH are for the special application area and should not be set.

(2) Make sure that the specified range does not overlap the no-protocol mode send area or the on-demand data area.

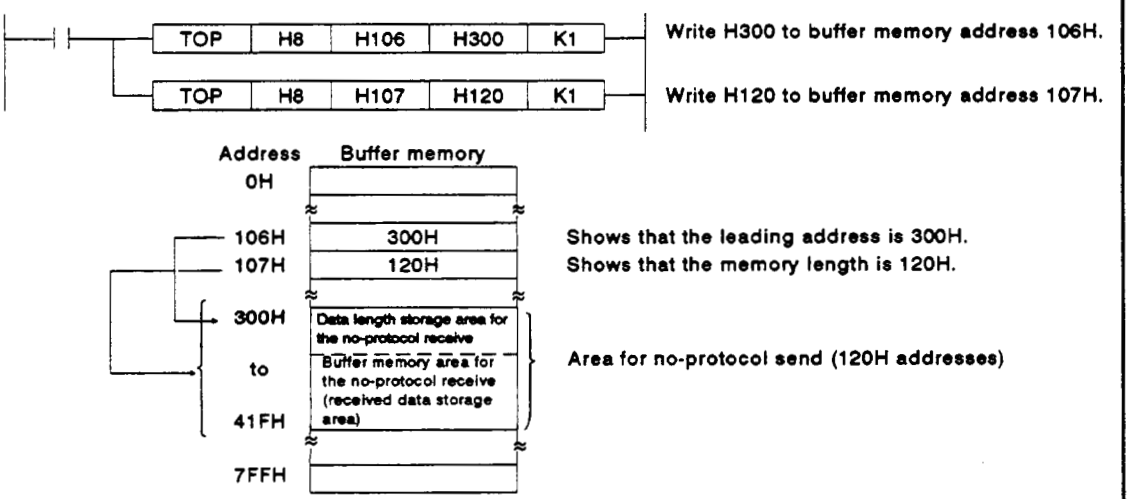
(3) Buffer memory address 107H should include the storage area of the no-protocol receive data length.

(4) If any range except the user area is set, the AJ71C24 will execute operations with defaults including the areas mentioned in (2) above.

Example

To set the head address to 300H and the memory size to 120H (AJ71C24 I/O addresses 80 to 9F)

(Sequence Program)



7.5 Settings in the Bidirectional Mode

This section describes how to set items in the bidirectional mode and gives examples.

The defaults set with the buffer memory section are for the no-protocol mode. When the interface mentioned in (1) is used in the no-protocol mode, all settings mentioned in this section are not necessary.

(1) Setting the bidirectional mode (address 112H)

When the mode setting switch (see Section 4.3.1) is set to "1" to "8", set the mode for the following interfaces to the bidirectional mode (see Section 4.3.1).

- When the mode switch setting is "1" to "4": RS-422 interface
- When the mode switch setting is "5" to "8": RS-232C interface

(2) Setting the time-out check time (address 113H)

Set the time-out check time which specifies the time from the beginning of data send to a computer connected through the bidirectional mode interface until the reception of the response message (see the figure in Section 10.5.1).

(3) Valid/invalid setting of data at simultaneous transmission (address 114H)

Set the data transmitted and received by the AJ71C24 to valid/invalid when a computer and the AJ71C24 begin simultaneously full-duplex send in the bidirectional mode (see Section 10.6).

(4) Setting the check sum enable/disable (address 115H)

Set whether the check sum code is added or not added to the message when transmitted between the AJ71C24 and a computer in the bidirectional mode. (see Section 10.5.2 (4)).

This setting is unrelated to the check sum setting (for dedicated protocol) with SW21 of the AJ71C24.

POINT

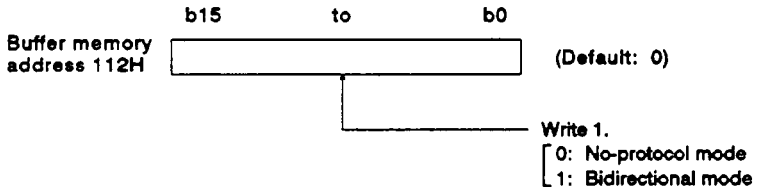
Sections 7.4.3 to 7.4.5 give the settings of the following areas used in the bidirectional mode. (Since the explanations in Sections 7.4.3 to 7.4.5 are for the no-protocol mode, change the mode from non-protocol to bidirectional when referring to these sections.)

- Bidirectional word/byte setting area: . . . . Section 7.4.3
- Bidirectional send area: . . . . . Section 7.4.4
- Bidirectional receive area: . . . . . Section 7.4.5

The mode with the dedicated protocol which is set with the mode setting switch is always valid for the interface set to the dedicated protocol.

Setting Method

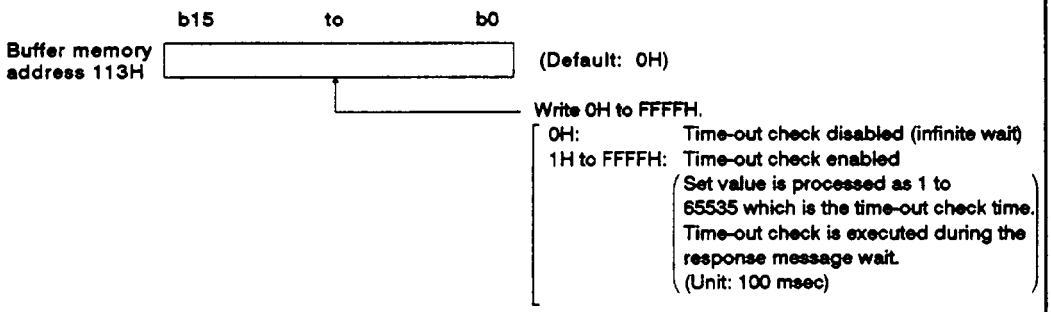
(1) Bidirectional mode



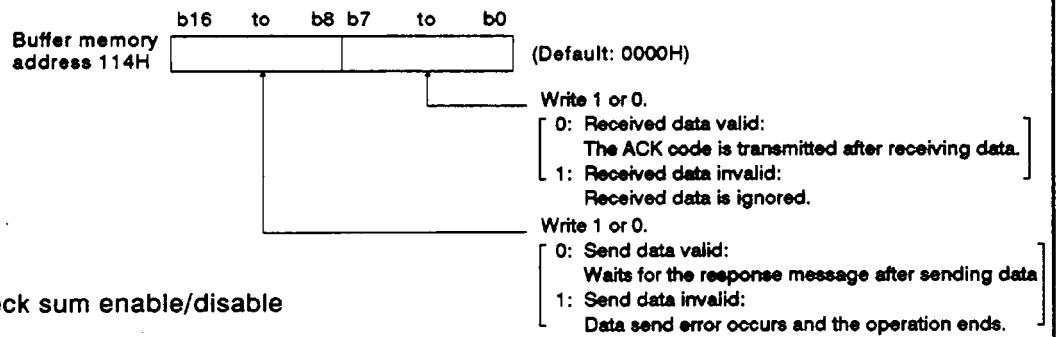
POINT

When the bidirectional mode is set, settings with buffer memory addresses 113H to 115H are valid.

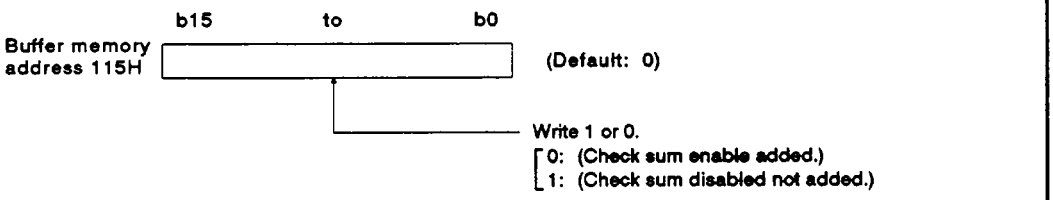
(2) Time-out check time


b15 to b0
Buffer memory address 113H
(Default: 0H)
Write 0H to FFFFH.
0H: Time-out check disabled (infinite wait)
1H to FFFFH: Time-out check enabled
Set value is processed as 1 to 65535 which is the time-out check time.
Time-out check is executed during the response message wait.
(Unit: 100 msec)

(3) Data valid/invalid at simultaneous transmission


b16 to b8 b7 to b0
Buffer memory address 114H
(Default: 0000H)
Write 1 or 0.
0: Received data valid:
The ACK code is transmitted after receiving data.
1: Received data invalid:
Received data is ignored.
Write 1 or 0.
0: Send data valid:
Waits for the response message after sending data
1: Send data invalid:
Data send error occurs and the operation ends.

(4) Check sum enable/disable



Setting Method

(1) Setting the bidirectional mode with the following conditions (AJ71C24 I/O addresses: 80 to 9F)

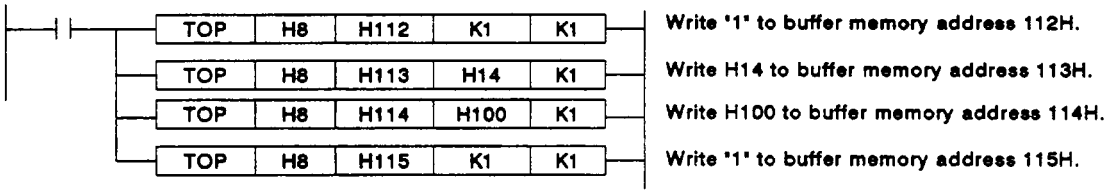
1) Set the bidirectional mode.

2) Set the time-out check time to 2 seconds. The setting value is 20 (14H).

3) Set the send data to "invalid" and the received data to "valid" for simultaneous transmission.

4) Set the check sum to "disable"

(Sequence Program)


TOP H8 H112 K1 K1
Write "1" to buffer memory address 112H.
TOP H8 H113 H14 K1
Write H14 to buffer memory address 113H.
TOP H8 H114 H100 K1
Write H100 to buffer memory address 114H.
TOP H8 H115 K1 K1
Write "1" to buffer memory address 115H.

(2) Setting the bidirectional mode with the following conditions (AJ71C24 I/O addresses: 110 to 12F)

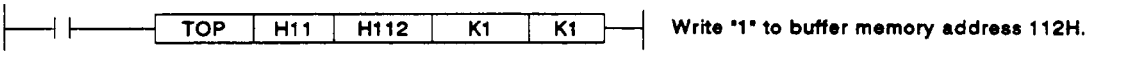
1) Set the bidirectional mode.

2) Set the time-out check time to "infinite".

3) Set the send data to "valid" and the received data to "valid" for simultaneous transmission.

4) Set the check sum to "enable".

(Sequence Program)



Leave settings of buffer memory addresses 113H for 115H for defaults.

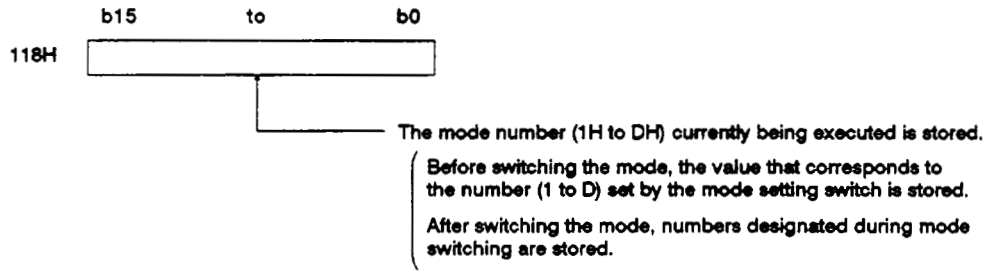
7.6 Mode Switch Setting

The following shows how to set items during mode switching and gives an example.

7.6.1 Reading in the mode setting state

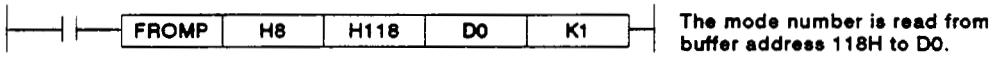
This section explains how to read a currently-executed mode number after the mode is switched.

Setting Method


b15
to
b0
118H
The mode number (1H to DH) currently being executed is stored.
Before switching the mode, the value that corresponds to the number (1 to D) set by the mode setting switch is stored.
After switching the mode, numbers designated during mode switching are stored.

Reading Example

To read the mode number currently being executed (AJ71C24 I/O addresses 80 to 9F)



REMARK

After switching the mode of the AJ71C24 (as explained in Section 7.6.2) the current mode number can be confirmed by reading the value in the designated mode-switching area (address 119H) of the buffer.

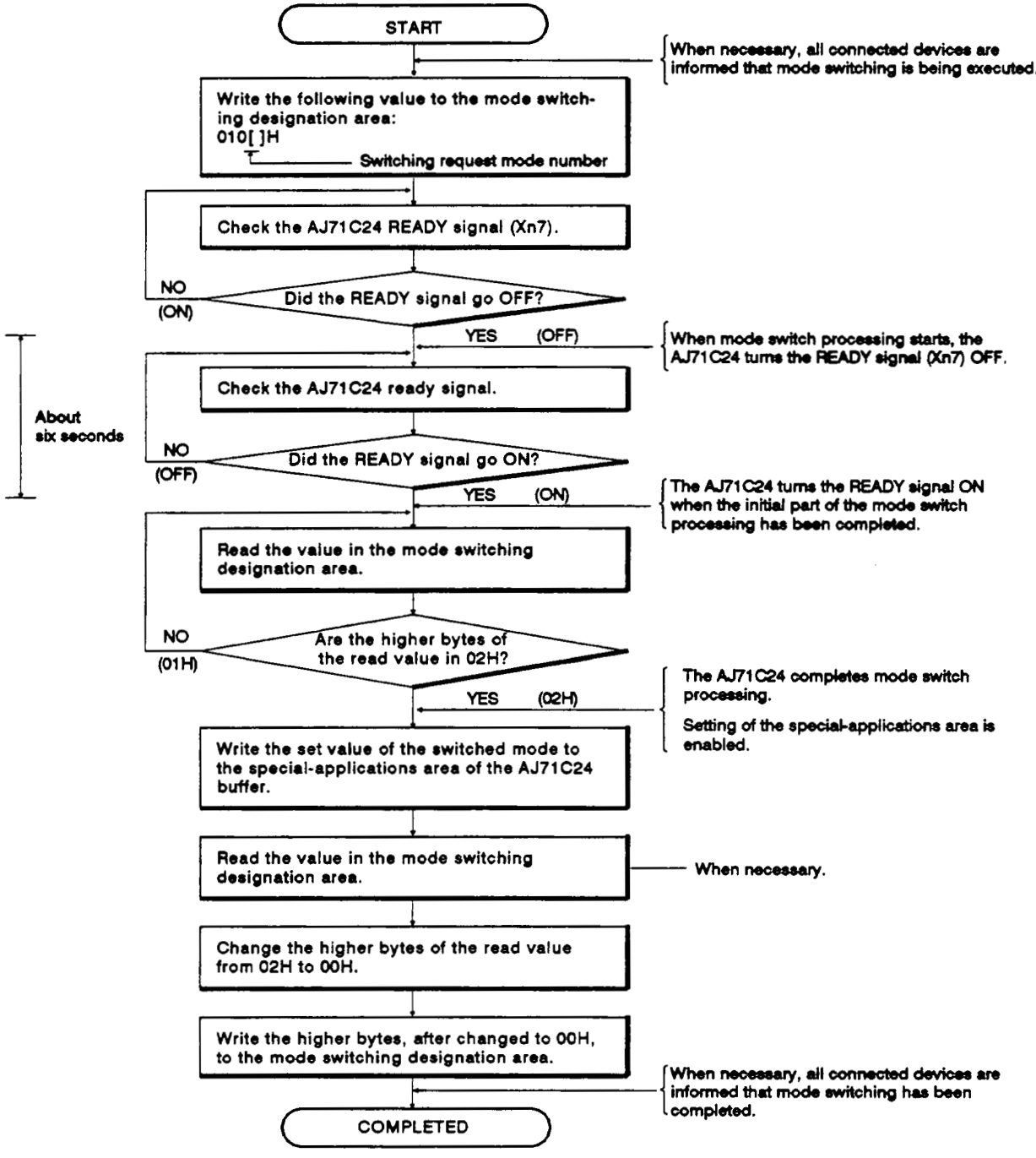
The lower four bits of the mode number are stored in 1H to DH.

7.6.2 Mode switching designation

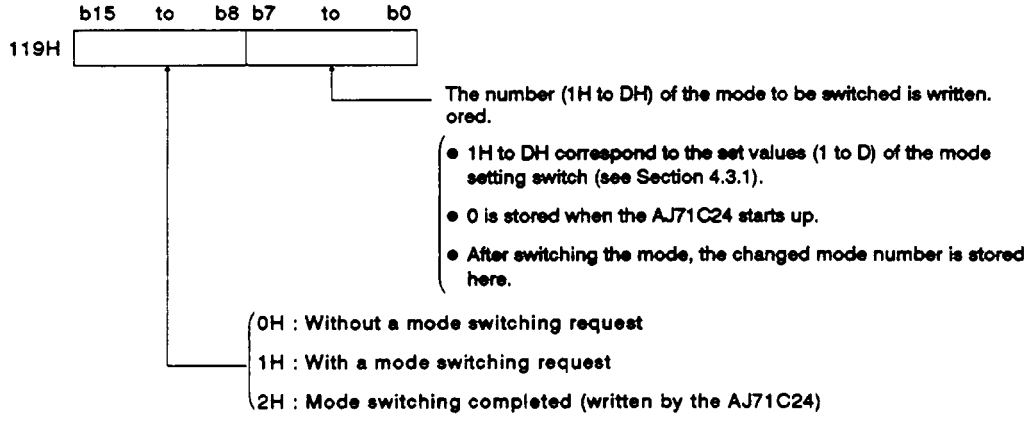
The following shows how to designate mode switching and gives an example of a sequence program.

This section explains how to specify the designated mode switching area (address 119H).

The following flowchart shows how to switch the mode.

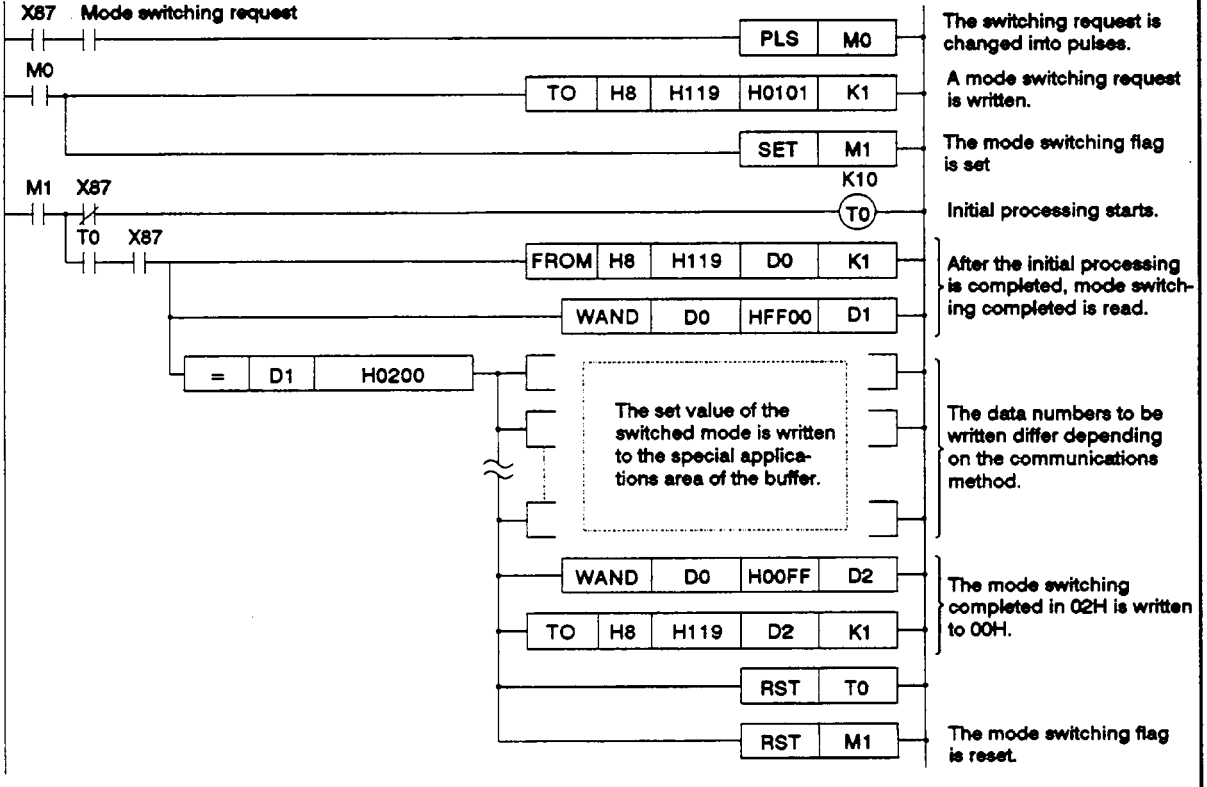

START
When necessary, all connected devices are informed that mode switching is being executed.
Write the following value to the mode switching designation area:
010[ ]H
Switching request mode number
Check the AJ71C24 READY signal (Xn7).
NO
(ON)
Did the READY signal go OFF?
YES (OFF)
When mode switch processing starts, the AJ71C24 turns the READY signal (Xn7) OFF.
About six seconds
Check the AJ71C24 ready signal.
NO
(OFF)
Did the READY signal go ON?
YES (ON)
The AJ71C24 turns the READY signal ON when the initial part of the mode switch processing has been completed.
Read the value in the mode switching designation area.
NO
(01H)
Are the higher bytes of the read value in 02H?
YES (02H)
The AJ71C24 completes mode switch processing.
Setting of the special-applications area is enabled.
Write the set value of the switched mode to the special-applications area of the AJ71C24 buffer.
Read the value in the mode switching designation area.
When necessary.
Change the higher bytes of the read value from 02H to 00H.
Write the higher bytes, after changed to 00H, to the mode switching designation area.
When necessary, all connected devices are informed that mode switching has been completed.
COMPLETED

Setting Method


b15 to b8 b7 to b0
119H
The number (1H to DH) of the mode to be switched is written. ored.
• 1H to DH correspond to the set values (1 to D) of the mode setting switch (see Section 4.3.1).
• 0 is stored when the AJ71C24 starts up.
• After switching the mode, the changed mode number is stored here.
0H : Without a mode switching request
1H : With a mode switching request
2H : Mode switching completed (written by the AJ71C24)

Example

when the mode is switched from a PC CPU to mode number 1 (AJ71C24 I/O addresses 80 to 9F)


X87 Mode switching request
PLS M0
The switching request is changed into pulses.
M0
TO H8 H119 H0101 K1
A mode switching request is written.
SET M1
The mode switching flag is set
M1 X87
K10
T0
Initial processing starts.
T0 X87
FROM H8 H119 D0 K1
WAND D0 HFF00 D1
After the initial processing is completed, mode switching completed is read.
= D1 H0200
The set value of the switched mode is written to the special applications area of the buffer.
The data numbers to be written differ depending on the communications method.
WAND D0 H00FF D2
TO H8 H119 D2 K1
The mode switching completed in 02H is written to 00H.
RST T0
RST M1
The mode switching flag is reset.

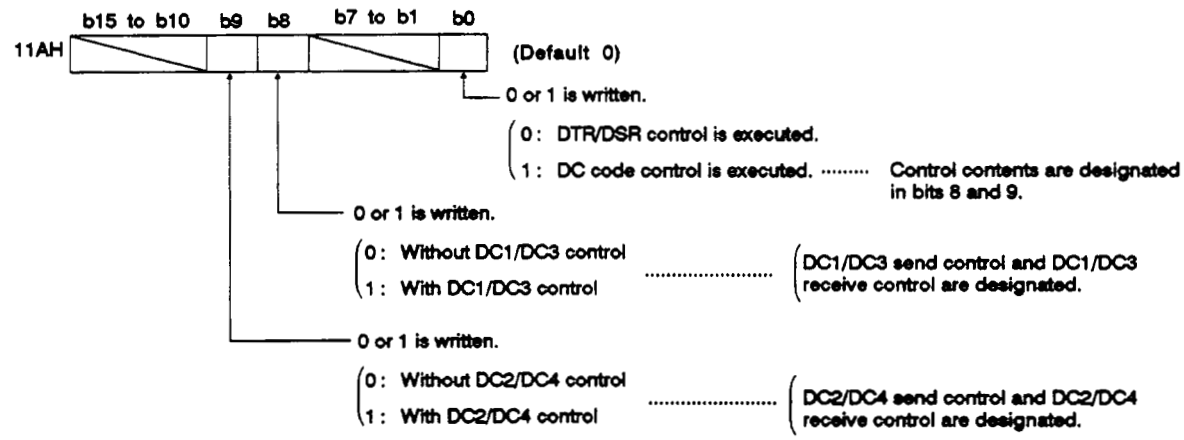
7.7 Transmission Control Setting

The following shows how to set items during transmission control and gives an example.

7.7.1 How to set transmission control

This section explains how to designate transmission control and gives an example of a sequence program.

Setting Method

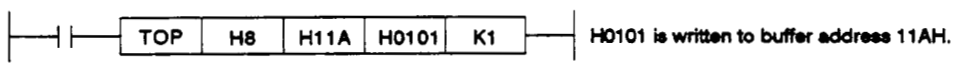

b15 to b10
b9
b8
b7 to b1
b0
11AH
(Default 0)
0 or 1 is written.
0 : DTR/DSR control is executed.
1 : DC code control is executed.
Control contents are designated in bits 8 and 9.
0 or 1 is written.
0 : Without DC1/DC3 control
1 : With DC1/DC3 control
DC1/DC3 send control and DC1/DC3 receive control are designated.
0 or 1 is written.
0 : Without DC2/DC4 control
1 : With DC2/DC4 control
DC2/DC4 send control and DC2/DC4 receive control are designated.

Example

(AJ71C24 I/O addresses 80 to 9F)

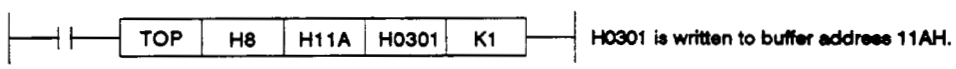
(1) When DC1/DC3 send control and receive control are executed

(Sequence program)



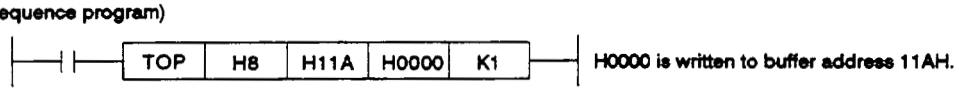
(2) When DC1/DC3 and DC2/DC4 send control and receive control are executed

(Sequence program)



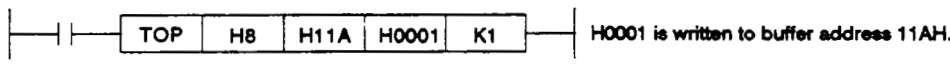
(3) When DTR/DSR control is executed

(Sequence program)



(4) When the transmission control function is not used

(Sequence program)



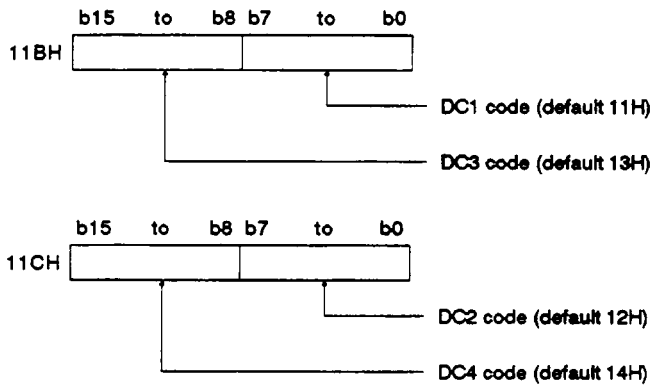
7.7.2 Settings for changing the addresses of DC1 to DC4 codes

This section describes how to change the addresses of DC1 to DC4 codes and gives an example of a sequence program.

When changing a DC code address, designate the corresponding DC code.

(Thus, when changing DC1, designate DC1 and DC3.)

Setting Method



POINT

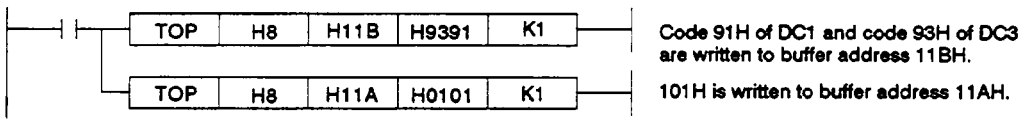
The DC1 to DC4 codes which are to be changed can be set in the range of 00H to FFH.

Example

(AJ71C24 I/O addresses 80 to 9F)

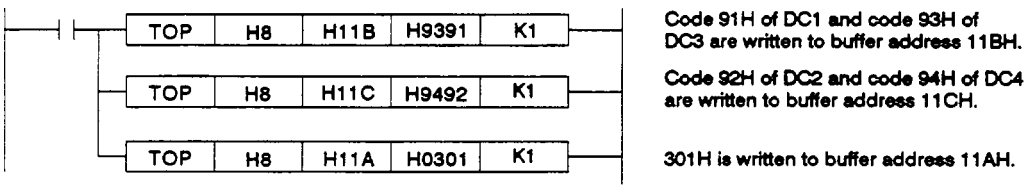
(1) To change the DC1 code address to 91H and the DC3 code address to 93H

(Sequence program)


TOP H8 H11B H9391 K1
Code 91H of DC1 and code 93H of DC3 are written to buffer address 11BH.
TOP H8 H11A H0101 K1
101H is written to buffer address 11AH.

(2) To change the DC1 to DC4 code addresses to 91H through 94H

(Sequence program)


TOP H8 H11B H9391 K1
Code 91H of DC1 and code 93H of DC3 are written to buffer address 11BH.
TOP H8 H11C H9492 K1
Code 92H of DC2 and code 94H of DC4 are written to buffer address 11CH.
TOP H8 H11A H0301 K1
301H is written to buffer address 11AH.

POINT

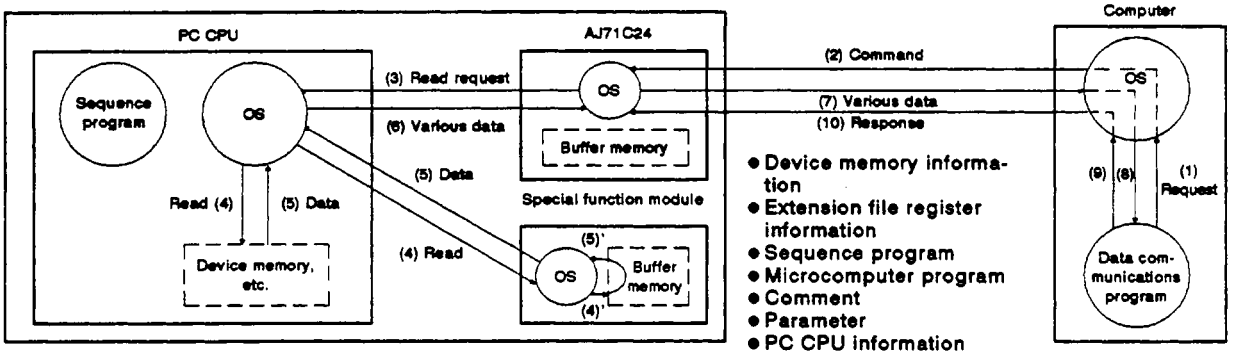
When changing the default values of DC codes, designate DC1/DC3 control and DC2/DC4 control to buffer address 11AH after changing the values in buffer addresses 11BH to 11CH.

8. COMMUNICATIONS USING DEDICATED PROTOCOLS

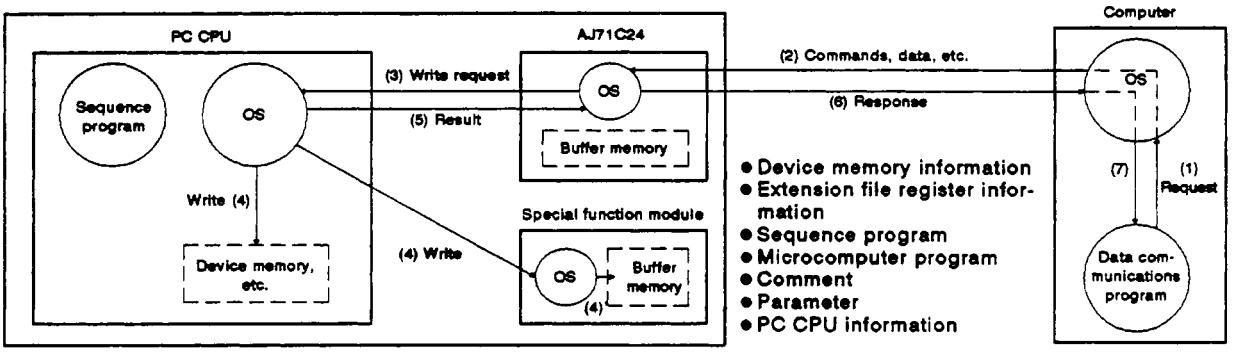
This chapter explains the details and methods of specifying control protocols 1 to 4 along with examples.

8.1 Data Flow in Communications with Dedicated Protocols

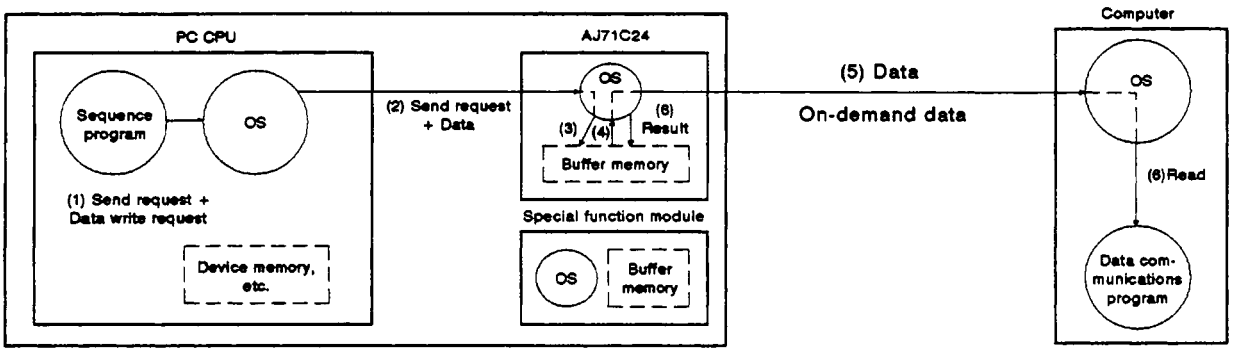
(1) The computer reads data from the PC CPU



(2) The computer sends data to the PC CPU



(3) The PC CPU sends data to the computer



REMARK

The OS (operating system) shown in the above illustrations is the software that uses resources such as the PC CPU, memory, terminals, files, and network efficiently.

In this manual, this software is described as the system program or system.

8.2 Programming Hints

8.2.1 To write data to the special use area in buffer memory

(1) Buffer memory is not backed up by a battery.

When the power is turned ON, the PC CPU is reset, or the mode is switched. all data in the buffer is set to default values. Therefore, whenever the power is turned ON, the CPU is reset, or the mode is switched, any data which has been changed from a default value must be written to the buffer.

(2) Except for the mode-switching area, data can only be written to the special applications area using the TO instruction in a sequence program. If data is written to the buffer memory using the command in a computer program, the AJ71C24 will not operate correctly. Never try to write data using a computer program.

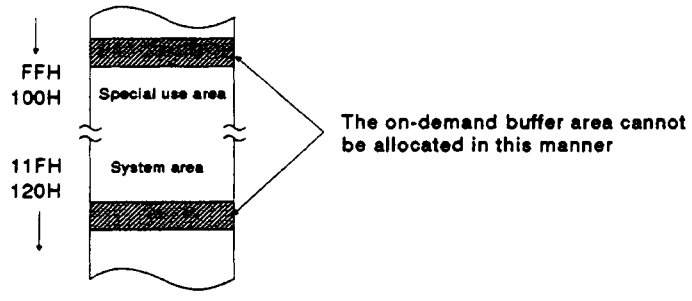
(3) If the following functions are used in combination with the dedicated protocol, make sure to allocate the user area in buffer memory so that the same area will not be used by different functions.

If the same area is allocated to different functions, the data in this area is rewritten and communications will not be correctly executed.

- No-protocol mode transmission or bidirectional mode transmission
- No-protocol mode receive or bidirectional mode receive
- Buffer memory read/write (CR/CW command) function
- On-demand function

The memory areas preceding and following the special use area cannot be allocated as a single area. The areas 0H to FFH and 120H to 7FFH must be recognized as independent areas.

Example:



(4) If the designation is made to process the send/receive data in the no-protocol mode or bidirectional mode in units of words or bytes, the on-demand data is processed in the same designated unit.

8.2.2 PC CPU operation during data communications

(1) PC CPU scan time

In response to the access request from the AJ71C24, the PC CPU processes only a single request in each END processing while the PC CPU is running.

Therefore, the scan time is extended by the time used for processing.

For intervening and processing times required for communications between the AJ71C24 and PC CPU, see Appendix 5.

The scan time is extended approximately 0.2 msec if an AJ71C24 is installed (0.1 msec for an A3H, A2A (S1), or A3ACPU), even if the PC CPU is not linked.

(2) Simultaneous access

Because the PC CPU executes only a single processing in END processing, if the PC CPU is accessed by more than one AJ71C24, access to the PC CPU is suspended until other processing is completed. Thus, the number of times scanning is done is increased.

8.2.3 Precautions during data communications

(1) The conditions under which the AJ71C24 transmission sequence is initialized are as follows:

- The power supply is turned ON, the PC CPU is reset with the reset switch, or the mode of the AJ71C24 is switched.
- Data communications is completed normally.
- The control code EOT or CL is received.
- The NAK control code is received.
- During full-duplex communications through the RS-232C interface, the CD signal is turned OFF.

  (The ON/OFF status of the CD signal is ignored if the CD terminal check function is disabled.)

(2) NULL code transmission from the AJ71C24

A framing error might occur in the AJ71C24 if nothing is sent from the computer to the AJ71C24 via the RS-422 interface. In this case, the AJ71C24 sends "00H" (NULL code) to the computer. These NULL codes should be ignored by the computer.

The computer should also ignore all data sent from the AJ71C24 prior to an STX, ACK, or NAK code.

(3) NAK response from the AJ71C24

The NAK response is given from the AJ71C24 to the computer using the dedicated protocol if an error is detected. Therefore, the NAK response may be output even while the computer is sending data in the full-duplex communications mode.

(4) Data link error processing

The AJ71C24 enters the standby state (see Section 3.6 I/O list for programmable controller CPU) if a data link error occurs during data communications with a PC CPU (the PC CPU number being other than FFH) on MELSECNET(II), MELSECNET/B.

If an error is detected by the computer when executing the time check, send a clear command (EOT or CL, see Section 8.4.5 (1)) to initialize the transmission sequence.

(5) Sending a command from the computer

When sending a command from the computer to the AJ71C24 using the dedicated protocol, send the command only after the data communications called by the preceding command is completed.

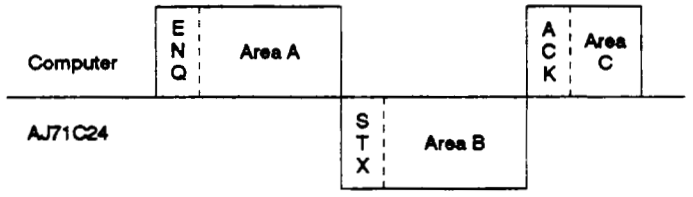
(6) Replacing a PC CPU on the data link system

After starting up the AJ71C24, if a PC CPU on the data link system is replaced by a different model PC CPU, start up the AJ71C24 again.

(First, reset the power supply to the self station's PC CPU, then reset the CPU, and then switch the mode of the AJ71C24.)

8.3 Basics of Dedicated Protocol Control Procedures

(1) Reading data by the computer from the AJ71C24



(a) Areas A and C indicate transmission from the external device to the AJ71C24.

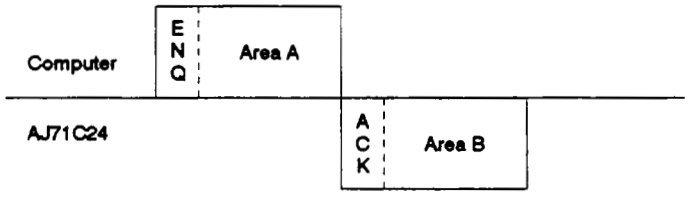
(b) Area B indicates transmission from the AJ71C24 to the external device.

(c) Computer programs are created so that all data is transmitted from left to right.

(Example: In area A, data is transmitted to the right after the ENQ signal.)

(d) Area C of the program completes data communications (whether communications are being carried out or not) and permits the next data communications to be carried out.

(2) Writing data by the computer to the AJ71C24



(a) Area A indicates transmission from the external device to the AJ71C24.

(b) Area B indicates transmission from the AJ71C24 to the external device.

(c) Computer programs are created so that all data is transmitted from left to right.

(Example: In Area A, data is transmitted to the right after the ENQ signal.)

8.4 Basic Formats of Dedicated Protocol

There are 4 formats of control protocol. Any of these formats can be designated by selecting the mode setting switch (Section 4.3.1) or mode number during mode switching. The differences between the control formats (based on format 1) are as follows:

Format 2 : Format 1 with block number added.

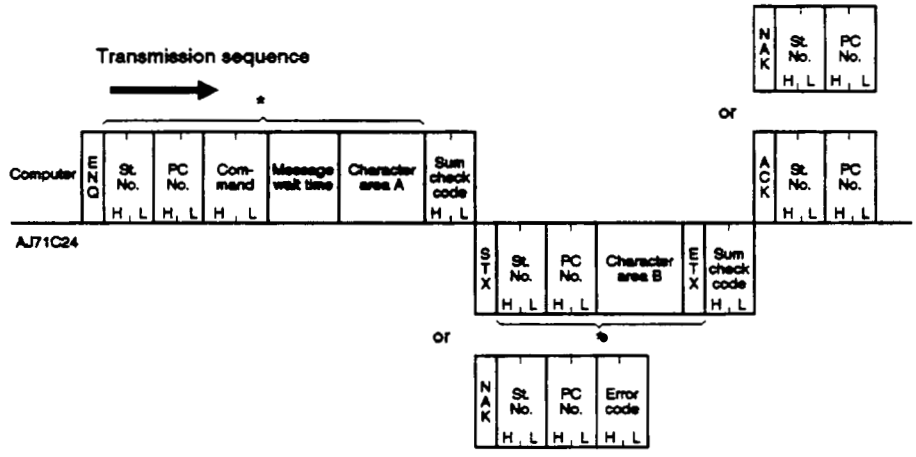
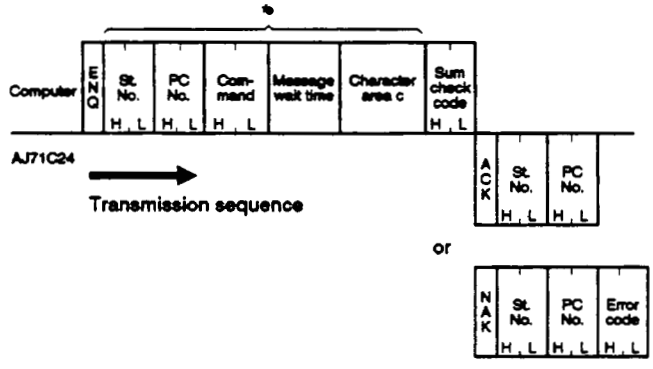
Format 3 : Format 1 with STX and ETX added.

Format 4 : Format 1 with CR and LF added.

The following sections describe details of the four control protocols and the meanings of individual items.

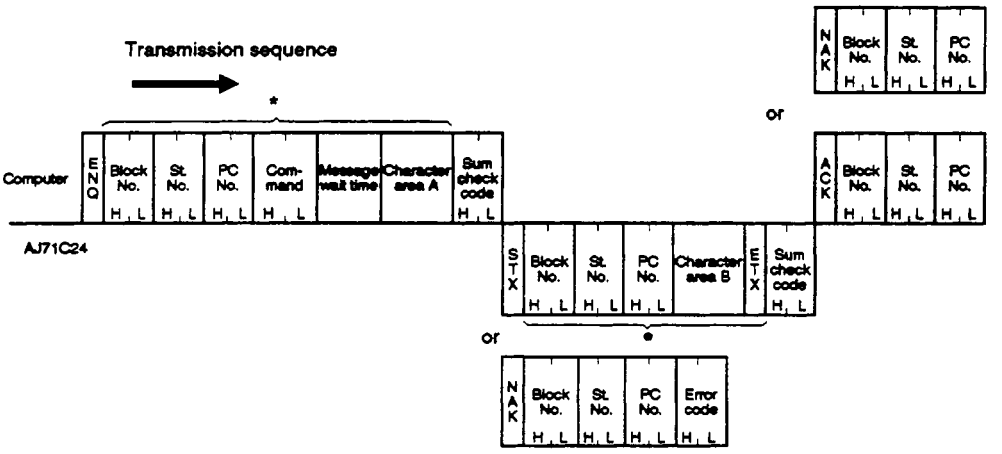
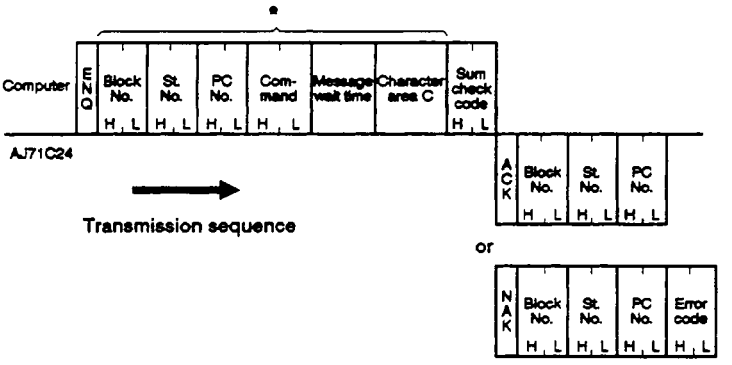
8.4.1 Control format 1

St. No. : Station number

Description	Control Protocol
To read data from the PC CPU to the computer	
To write data from the computer to the PC CPU	
Remarks	(1) The sum check is enabled by DIP switch 21. The sum check code only exists when the sum check is enabled by turning DIP switch 21 ON. (2) The sum check is made for characters marked "*" in these diagrams. (3) In these diagrams, the contents of "character area A", "character area B", and "character area C" depend on the individual system. For details, see the relevant sections. The contents of all character areas are the same for all 4 formats.

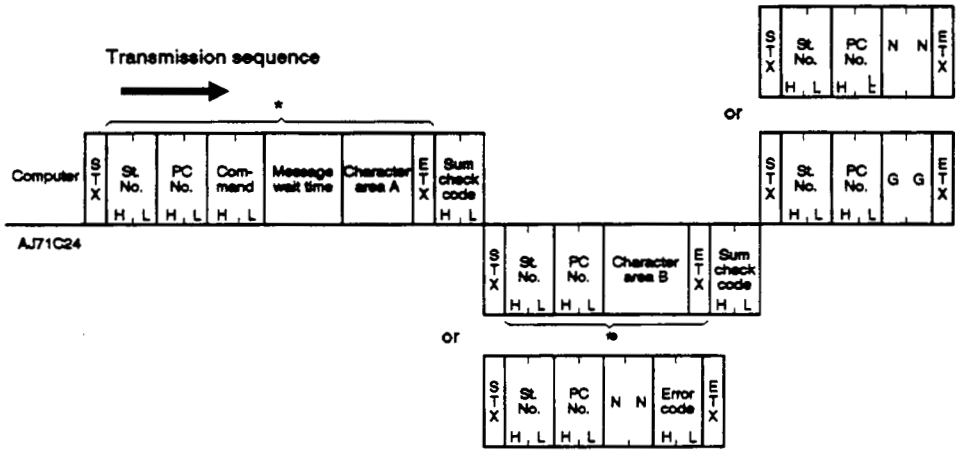
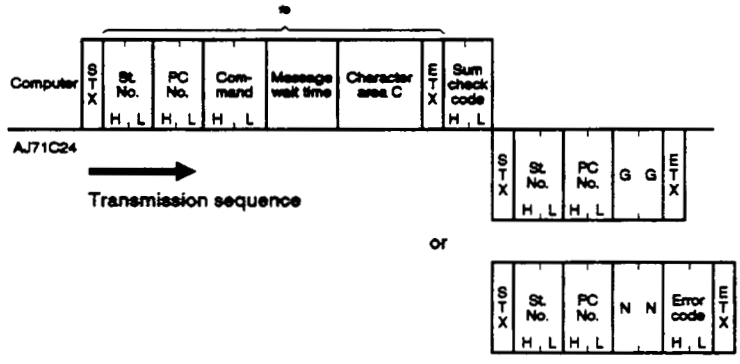
8.4.2 Control format 2

St. No. : Station number

Description	Control Protocol
To read data from the PC CPU to the computer	
To write data from the computer to the PC CPU	
Remarks	(1) The sum check is enabled by DIP switch 21. The sum check code only exists when the sum check is enabled by turning DIP switch 21 ON. (2) The sum check is made for characters marked "*" in these diagrams. (3) In these diagrams, the contents of "character area A", "character area B", and "character area C" depend on the individual system. For details, see the relevant sections. The contents of all character areas are the same for all 4 formats.

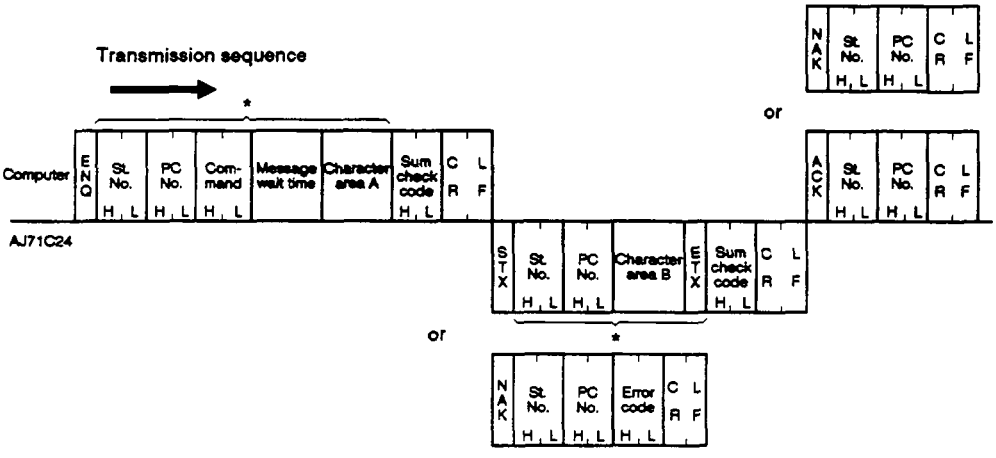
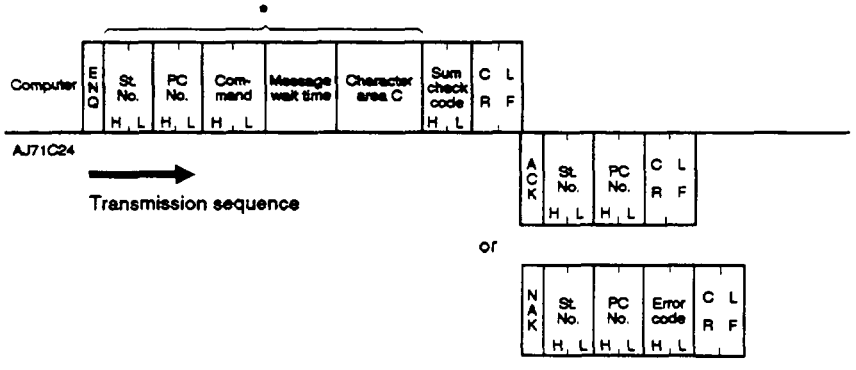
8.4.3 Control format 3

St. No. : Station number

Description	Control Protocol
To read data from the PC CPU to the computer	
To write data from the computer to the PC CPU	
Remarks	(1) The sum check is enabled by DIP switch 21. The sum check code only exists when the sum check is enabled by turning DIP switch 21 ON. (2) The sum check is made for characters marked "*" in these diagrams. (3) In these diagrams, the contents of "character area A", "character area B", and "character area C" depend on the individual system. For details, see the relevant sections. The contents of all character areas are the same for all 4 formats.

8.4.4 Control format 4

St. No. : Station number

Description	Control Protocol
To read data from the PC CPU to the computer	
To write data from the computer to the PC CPU	
Remarks	(1) The sum check is enabled by DIP switch 21. The sum check code only exists when the sum check is enabled by turning DIP switch 21 ON. (2) The sum check is made for characters marked "*" in these diagrams. (3) In these diagrams, the contents of "character area A", "character area B", and "character area C" depend on the individual system. For details, see the relevant sections. The contents of all character areas are the same for all 4 formats.

8.4.5 Setting protocol data

(1) Control code

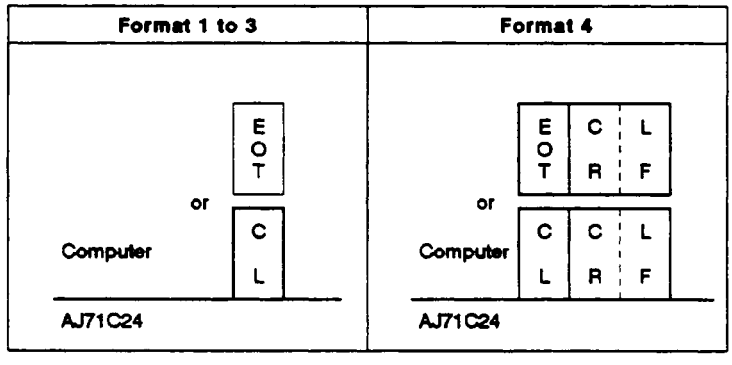
All control codes are sent and received in hexadecimal. They are shown in the following table.

Signal	Code (Hexadecimal)	Description	Signal	Code (Hexadecimal)	Description
NUL	00H	Null	LF	0AH	Line Feed
STX	02H	Start of Text	CL	0CH	Clear
ETX	03H	End of Text	CR	0DH	Carriage Return
EOT	04H	End of Transmission	NAK	15H	Negative Acknowledge
ENQ	05H	Enquiry	G	47H	Good
ACK	06H	Acknowledge	N	4EH	No Good

(a) The NUL code (00H) is ignored in all messages. If a NUL code is included in a message, it is processed as if it did not exist.

(b) In format 3, control code "GG" is equivalent to ACK and "NN" is equivalent to NAK.

(c) After receiving an EOT or CL code, the AJ71C24 initializes transmission but does not answer. The initializing code depends on the format as indicated below. At this time there is no answer from the AJ71C24.



(2) Block number

The block number is an optional number assigned as a data reference number for the computer. Block numbers are used to arrange data, etc. Block numbers may be from 00H to FFH in 2-digit ASCII (hexadecimal).

(3) Station number

The station number is set by the station number setting switch on the front of the AJ71C24. It identify file which AJ71C24 in a station to access.

Station numbers must be in the range of 00H to 1FH (0 to 31) in 2-digit ASCII (hexadecimal).

POINTS

(1) The station number setting switch is set to a decimal value, but the station number is specified in hexadecimal. Example: Switch setting "10" corresponds to station number "0AH" specified in the protocol.

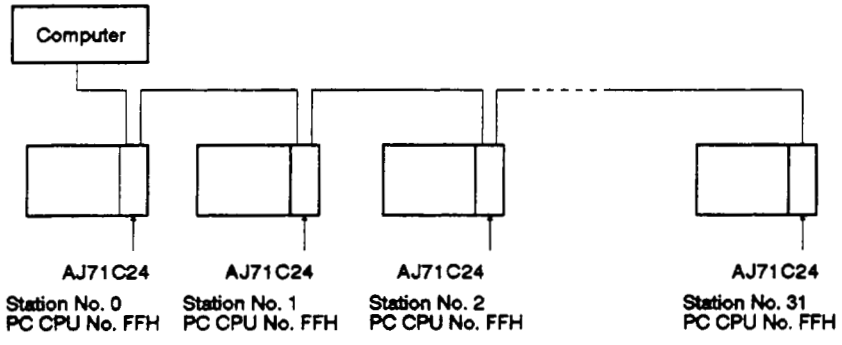
(2) For the global operation, specify station number "FFH". If 0 to 31 (00H to 1FH) is specified, "Xn2" turns ON at that station number only. For details, see Section 8.13.

(3) To execute data communications between the computers in the m:n multi-drop link, set the station number at the computer side in the range of 128 to 159 (80H to 9FH).

In this setting, the station numbers are determined according to the rule set by the computers.

For details, see Section 6.2.1.

Example:



REMARK

Station numbers do not need to be sequential.

(4) PC CPU number

The PC CPU number determines which PC CPU on MELSECNET(II), MELSECNET/B to access.

The PC CPU number may be from 00H to 40H/20H (00 to 64/32) in 2-digit ASCII (hexadecimal).

(a) Accessing PC CPUs equipped with AJ71C24 to which a computer is connected

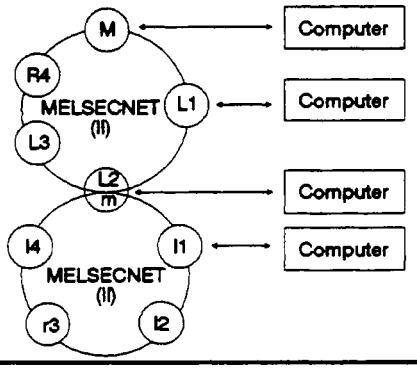
Set all PC CPU numbers to FF (self) using the computer. Use any function except the on-demand function.

(b) Accessing PC CPUs on MELSECNET(II), MELSECNET/B equipped with AJ71C24

1) When computer and master station are connecterd MELSECNET(II) local and remote I/O stations MELSECNET/B local stations: Set each slave link station number (1 to 64/32) in hexadecimal (01H to 40H/20H)

2) When computer and local station are connected MELSECNET(II) master stations, MELSECNET/B master stations: Set the PC CPU number to 00H

(c) The range of PC CPUs which can be accessed by setting the PC CPU numbers is shown below.



M.....Master station (1st tier)
L1.....Local station (2nd tier)
L2/m ....Local station (2nd tier)
Master station
L3.....Local station (2nd tier)
R4 .....Remote I/O station (2nd tier)
I1.....Local station (3rd tier)
I2.....Local station (3rd tier)
r3 .....Remote I/O station (3rd tier)
I4.....Local station (3rd tier)

PC CPU loaded with AJ71C24 connected to computer	PC CPUs to which a link is possible (PC CPU number)									
	Self (FF)	M (0)	L1 (1)	L2/m (2/0)	L3 (3)	R4 (4)	I1 (1)	I2 (2)	r3 (3)	I4 (4)
M	o	–	o	o	o	o *1	x	x	x	x
L1	o	o	–	x	x	x	x	x	x	x
L2/m	o	o	x	–	x	x	o	o	o *1	o
I1	o	x	x	o	x	x	–	x	x	x

o	Access to all devices possible by setting appropriate PC CPU numbers
o *1	Access to special-function module buffer memory possible by setting appropriate PC CPU numbers

POINT

If MELSECNET(II) is replaced by MELSECNET/B in either tier, the range of PC CPUs which can be accessed remains the same.

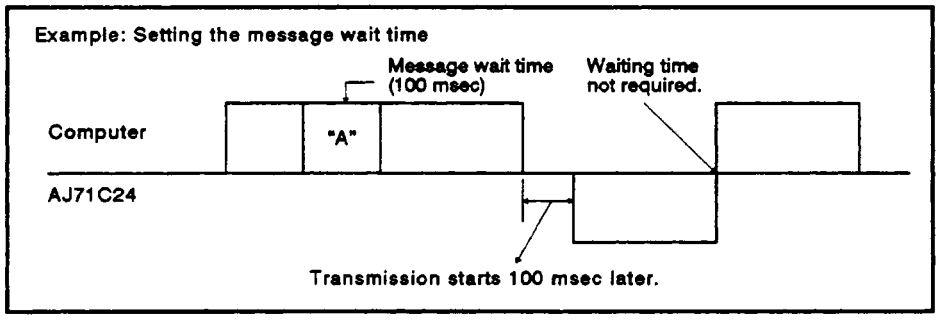
(5) Command

Used to specify the operation required, e.g. read, write, etc. Commands must be in 2-digit ASCII.

(6) Message wait time

This is a time delay required for some computers to switch from send to receive states. The message wait time determines the minimum waiting time before the AJ71C24 sends data after receiving it from the computer. Set this time in accordance with the computer specifications.

The message wait time may be set between 0 and 150 msec in units of 10 msec. The time is set from 0H to FH (0 to 15) in 1-digit hexadecimal, where 1 corresponds to 10 msec,

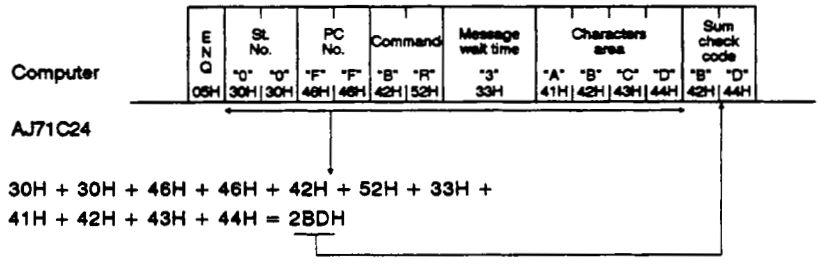


(7) Sum check code

The sum check code is 2-digit ASCII representing the lower 1 byte (8 bits) of the sum derived from the BIN code representing the checked data.

With DIP switch SW21 OFF, the sum check code is not added.

Example: If A,B,C, and D are transferred in format 1, setting station number 0, PC CPU number FF, command BR (batch read of device memory), and message wait time to 30 msec, the sum check code value is as shown below

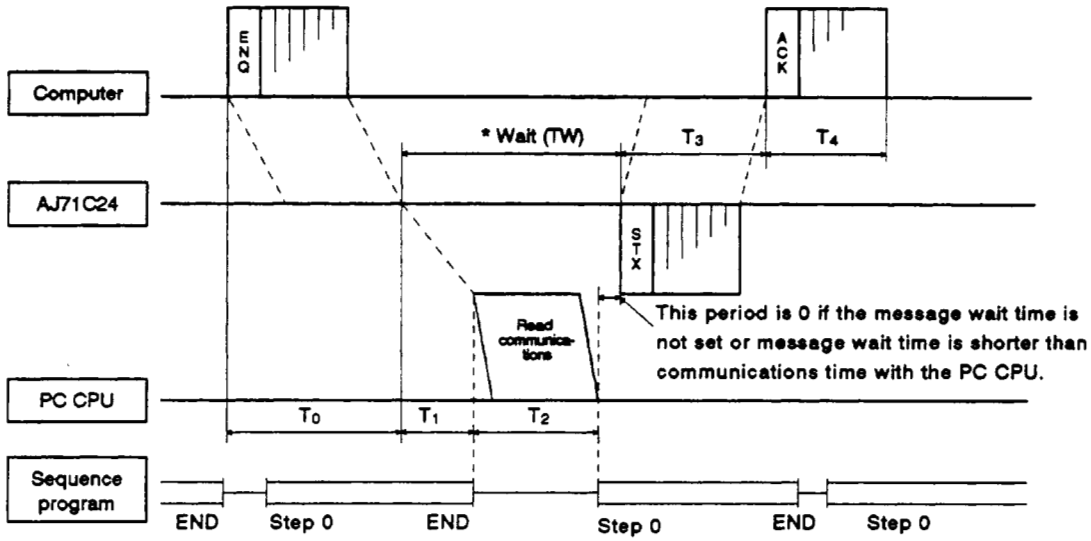


(8) Error code

- Indicates an error following a NAK transmission.
- Error codes are transmitted as 2-digit ASCII (hexadecimal) in the range of 00H to FFH.
- If two or more errors occur simultaneously, the error code of the lowest number is transmitted.
- For error code details, see Section 11.1.

8.5 Transmission Sequence Timing Charts and Communications Time

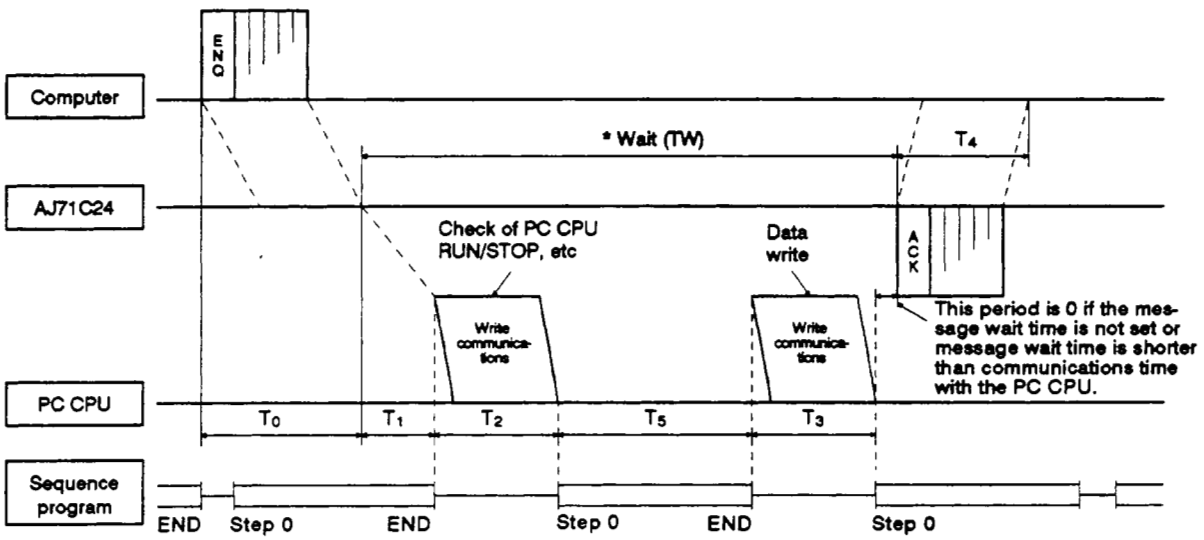
(1) To read data from the PC CPU to the computer
("*" indicates that the message wait time has been set.)



REMARK

For file register and parameter, an extra 1 scan plus T2 is required.

(2) To write data from the computer to the PC CPU
("*" indicates that message wait time has been set.)



REMARK

As shown above, communications between the AJ71C24 and the PC CPU is always made after END. Therefore, the scan time is extended by the time used for communications.

Appendix 5 gives the communications time.

Section 3.3.1 gives the number of points processed per communication after END.

(3) Communications time

This section describes how to calculate approximate communications time from the start of data transmission from the computer to the completion of all communications after a reply is sent from the AJ71C24.

For T0 to T4, see (1) and (2) on the previous page.

(a) To read data from the PC CPU to the computer

Communications time = T0 + (longer time of T1 + T2 or TW) + T3 + T4

where,

T0, T3, T4 = 1/baud rate X the number of bits per character
(1 + 7/8 + 0/1 + 1/2) x the character length
- Start bit
- Data length (7 or 8)
- Parity bit (0 or 1)
- Stop bit (1 or 2)

T1 = maximum 1 scan time (since data entry to the PC CPU is made after END processing. If the PC CPU is not running, T1 is 0.)

T2 = value in Appendix 5

TW = message wait time

(b) To write data from the computer to the PC CPU

Communications time = T0 + (longer time of T1 + T2+ T3 + T5 or TW) + T4

where,

T0, T4 = 1/baud rate X the number of bits per character
(1 + 7/8 + 0/1 + 1/2) x the character length
- Start bit
- Data length (7 or 8)
- Parity bit (0 or 1)
- Stop bit (1 or 2)

T1 = maximum 1 scan time (since data entry to the PC CPU is made after END processing. If the PC CPU is not running, T1 is 0.)

T2, T3 = value in Appendix 5
(For functions processed in 1 scan, T3 is 0.)

TW = message wait time

T5 = 1 scan time
(For functions processed in one scan, T5 is 0.)

(4) Transmission time through Data link systems

(a) The transmission time (T1) for data transmission by specifying the PC CPU number to a PC CPU on MELSECNET(II), MELSECNET/B not equipped with an AJ71C24 is calculated as follows:

- Local station

  Transmission time (T1) = (Transmission delay time A *1 + scan time for station 1 loaded with AJ71C24) × 2 *2

- Remote station

  Transmission time (T1) = (Transmission delay time B *1 + MELSECNET master station scan time) × 2 *2

*1 See the sections of the Data Link Reference Manual that explain corresponding data link system transmission delay times.
Transmission delay time A
See the table which describes LRDP instruction processing time.
Transmission delay time B
See the table which describes RFRP instruction processing time.

*2 Substitute "x 3" for "x 2" in the above equations for the first data communications after the power supply to the relevant station has been turned ON after the PC CPU has been reset.
If fewer than 11 stations are communicating, substitute (x 1 for x 2) for the second (and subsequent) communications.

Example:

The transmission time for α MELSECNET master station equipped with AJ71C24 to read a local station device memory:

(Conditions: L<LS<M, M : 80 msec α1 : 10 msec)

Transmission time T1 = (M x 4 + α1 x 4 + M) x 2
= (80 x 4 + 10 x 4 + 80) x 2 = 880

The transmission time is 880 msec. Where:

M : MELSECNET master station scan time

α1 : MELSECNET master station link refresh time

LS : Link scan time

L : MELSECNET local station scan time

- Causes of delayed transmission time (T1)

  Instructions requiring 2 scans for transmission (writing to device "R", etc.) need double the time derived from the equations above.

  When other stations in the link are being monitored by an A6GPP, the transmission time doubles for each station to be monitored.

  The Data Link Reference Manual gives details of the data link.

POINT

Under some conditions, data transmission to a PC CPU on MELSECNET(II), MELSECNET/B not equipped with an AJ71C24 can cause a considerable time delay.

This time delay can be reduced by carrying out all communications from the computer to PC CPUs to stations equipped with an AJ71C24 (PC CPU station number FFH) and all other data communications using the data link (B, W).

8.6 Character Area Data Transmission

The concept of transmission data handled as character areas when using commands to carry out data communications between the computer and the PC CPU is explained in this section. The data shown in the examples is contained in character area B in the case of read and monitor, and in character area C in the case of write, test, and monitor data register.

(1) Bit device memory read and write

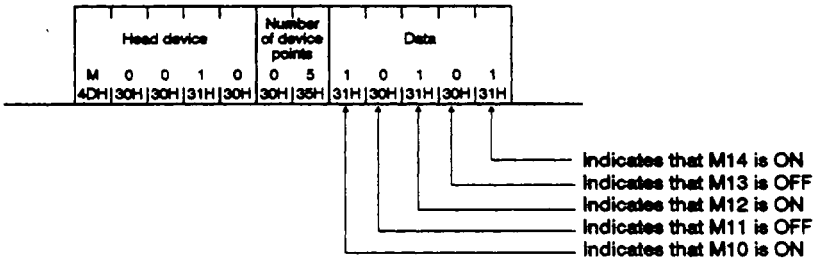
The bit device memory can be handled in bit units (1 device point) or word units (16 device points).

These units are described below.

(a) Bit units (1 point)

When the bit device memory is handled as bit units, the specified number of device points from the specified head device in sequence from the left are represented as 1 (31H) if the device is ON, or 0 (30H) if the device is OFF.

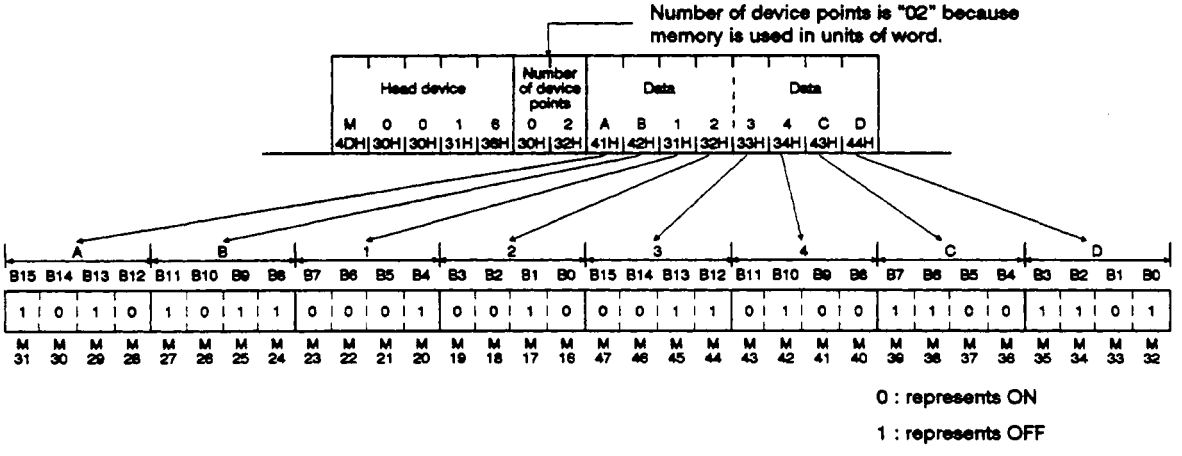
Example: Indication of the ON/OFF status of 5 points from M10


Head device
Number of device points
Data
M 0 0 1 0
0 5
1 0 1 0 1
4DH 30H 30H 31H 30H
30H 35H
31H 30H 31H 30H 31H
Indicates that M14 is ON
Indicates that M13 is OFF
Indicates that M12 is ON
Indicates that M11 is OFF
Indicates that M10 is ON

(b) Word units (16 points)

When the bit device memory is handled as word units, each word is expressed sequentially in hexadecimal values in 4-bit units from the higher bit.

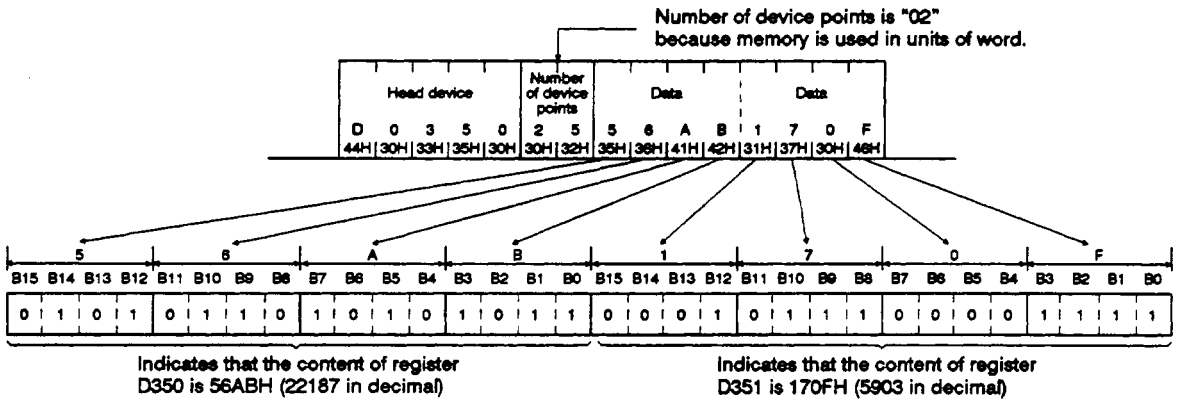
Example: Indication of the ON/OFF status of 32 points from M16


Number of device points is "02" because memory is used in units of word.
Head device
Number of device points
Data
Data
M 0 0 1 6
0 2
A B 1 2
3 4 C D
4DH 30H 30H 31H 36H
30H 32H
41H 42H 31H 32H 33H 34H 43H 44H
A B 1 2 3 4 C D
B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
1 0 1 0 1 0 1 1 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 1 1 0 0 1 1 0 1
M31 M30 M29 M28 M27 M26 M25 M24 M23 M22 M21 M20 M19 M18 M17 M16 M47 M46 M45 M44 M43 M42 M41 M40 M39 M38 M37 M36 M35 M34 M33 M32
0 : represents ON
1 : represents OFF

(2) Word device memory read and write

In the word device memory, each word is expressed sequentially in hexadecimal values in 4-bit units from the higher bit.

Example: Indication of the contents of the D350 and D351 registers


Number of device points is "02"
because memory is used in units of word.
Head device
Number of device points
Data
Data
D 0 3 5 0
44H 30H 33H 35H 30H
2 5
30H 32H
5 6 A B
35H 36H 41H 42H
1 7 0 F
31H 37H 30H 46H
5 6 A B 1 7 0 F
B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
0 1 0 1 0 1 1 0 1 0 1 0 1 0 1 1
0 0 0 1 0 1 1 1 0 0 0 0 1 1 1 1
Indicates that the content of register D350 is 56ABH (22187 in decimal)
Indicates that the content of register D351 is 170FH (5903 in decimal)

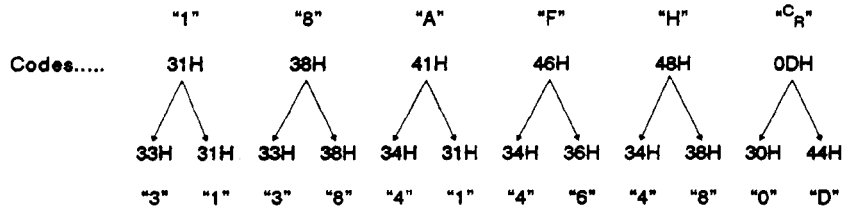
REMARK

(1) Extension file memory read and write, buffer memory read and write, and on-demand data when word units are specified are handled according to the same principle as the word device memory.

(2) To output a character-string with the PR instruction externally after transmitting it from the computer to the PC CPU, the processing should be as shown below:

1) The character-string to be transmitted is developed into 2-byte codes in units of characters.

Example: To transmit "18AFH $^{C}_{R}$" to a sequence program.



2) The character-string developed into 2-byte codes is arranged in units of 2 characters and sent to the AJ71C24.

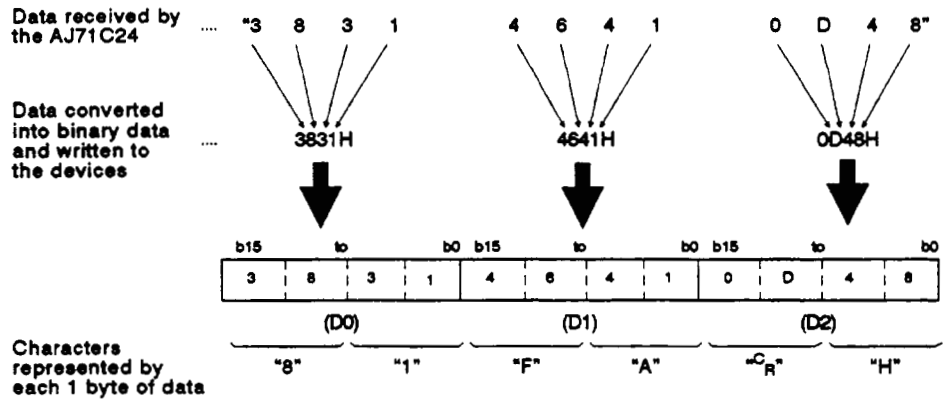
Example: The character-string used in the above example in 1.

"31 38 41 46 48 0D" "383146410D48"

"383146410D48" is sent from the computer to the AJ71C24.

The AJ71C24 converts the data sent from the computer into binary data and writes it to the designated device.

Example: To write the data composed in the above example in 2) to D0 to D2 in the PC CPU.



8.7 Device Memory Read/Write

8.7.1 Commands and device ranges

(1) The ACPU common commands and device ranges used for device memory read/write are described below.

(a) ACPU common commands

Item		Command: Symbol	Command: ASCII Code	Processing Contents	Number of Points Processed per Communications	PC CPU Status: During STOP	PC CPU Status: During RUN: SW22 ON	PC CPU Status: During RUN: SW22 OFF
Batch Read	Bit units	BR	42H, 52H	Reads bit devices (X, Y, M, etc.) in units of points.	256 points	o	o	o
	Word units	WR	57H, 52H	Reads bit devices (X, Y, M, etc.) in units of 16 points.	32 words (512 points)			
				Reads word devices (D, R, T, C, etc.) in units of points.	64 points			
Batch Write	Bit units	BW	42H, 57H	Writes data to bit devices (X, Y, M, etc.) in units of points.	160 points	o	o	x
	Word units	WW	57H, 57H	Writes data to bit devices (X, Y, M, etc.) in units of 16 points.	10 words (160 points)			
				Writes data to word devices (D, R, T, C, etc.) in units of points.	64 points			
Test (Random Write)	Bit units	BT	42H, 54H	Sets/resets bit devices (X, Y, M, etc.) in units of points by designating the devices and device numbers at random.	20 points	o	o	x
	Word units	WT	57H, 54H	Sets/resets bit devices (X, Y, M, etc.) in units of 16 points by designating the devices and device numbers at random.	10 words (160 points)			
				Writes data to word devices (D, R, T, C, etc.) in units of points by designating the devices and device numbers at random.	10 points			
Monitor Data Registration	Bit units	BM	42H, 4DH	Sets the bit devices (X, Y, M, etc.) to be monitored in units of points.	40 points*	o	o	o
	Word units	WM	57H, 4DH	Sets the bit devices (X, Y, M, etc.) to be monitored in units of 16 points.	20 words* (320 points)			
				Sets the word devices (D, R, T, C, etc.) to be monitored in units of points.	20 points			
Monitor	Bit units	MB	4DH, 42H	Monitors the devices registered for monitoring.	—	o	o	o
	Word units	MN	4DH, 4EH					

Note : o ..... Executable

x ..... Not executable

For the number of processing points indicated by an asterisk (*), the number is one half of the values indicated in the table for the input device (x) when PC CPUs other than the A3H CPU, A2ACPU(S1), and A3ACPU are used. (See *1 in 3.3.1 (1).)

POINT

When ACPU common commands are used to access the devices in an A2ACPU(S1) or A3ACPU, the device number ranges described in (b) can be used.

Use the AnACPU dedicated commands described in (2) to access the extension devices.

(b) Device ranges when ACPU common commands are used

The devices and device number ranges that can be used for the device memory access operation are described below.

The device designation code consists of 5 characters.

Leading zeros in the device number (underlined zeros in X0070, for example) can be expressed with a blank code (20H).

Device	+	Device number	=5 characters
{ 1 character (2 characters for T/C) }		{ 4 characters (3 characters for T/C) }	

Bit Device			Word Device		
Device	Device Number Ranges (Characters)	Decimal/ Hexadecimal Expression	Device	Device Number Range (Characters)	Decimal/ Hexadecimal Expression
Input X	X0000 to X07FF	Hexadecimal	Timer (present value) T	TN000 to TN255	Decimal
Output Y	Y0000 to Y07FF	Hexadecimal	Counter (present value) C	CN000 to CN255	Decimal
Internal relay M	M0000 to M2047	Decimal	Data register D	D0000 to D1023	Decimal
Latch relay L	L0000 to L2047	Decimal	Link register W	W0000 to W03FF	Hexadecimal
Step relay S	S0000 to S2047	Decimal	File register R	R0000 to R8191	Decimal
Link relay B	B0000 to B03FF	Hexadecimal	Special register D	D9000 to D9255	Decimal
Annunciator F	F0000 to F0255	Decimal			
Special relay M	M9000 to M9255				
Timer (contact) T	TS000 to TS255				
Timer (coil) T	TC000 to TC255				
Counter (contact) C	CS000 to CS255				
Counter (coil) C	CC000 to CC255				

POINTS

(1) To designate the bit device ranges in units of words, the bit device number must be a multiple of 16.

(2) Although the ranges are designated for M, L, and S, if the range for M is designated by L or S, the same processing occurs. This is also true for the ranges for L and S.

(3) The ranges of special relays (M9000 to M9255) and special registers (D9000 to D9255) are divided into the areas for read only, write only, and system use.

Trying to write data to the ranges outside the write-only area might cause the PC CPU to malfunction.

The ACPU programming manual gives details concerning special relays and special registers.

(4) When using an extension file register to read/write file register data from/to a PC CPU, use the commands explained in Section 8.8 for file register (R) read/write operations, use the commands explained in Section 8.8 for read and write operations for the file register (R).

(2) The AnACPU dedicated commands and device ranges used for device memory read/write are described below.

(a) AnACPU dedicated commands

Item		Command		Processing Contents	Number of Points Processed per Communications	PC CPU Status		
		Symbol	ASCII Code			During STOP	During RUN	
							SW22 ON	SW22 OFF
Batch Read	Bit units	JR	4AH, 52H	Reads bit devices (X, Y, M, etc.) in units of points.	256 points	o	o	o
	Word units	QR	51H, 52H	Reads bit devices (X, Y, M, etc.) in units of 16 points.	32 words (512 points)			
				Reads word devices (D, R, T, C, etc.) in units of points.	64 points			
Batch Write	Bit units	JW	4AH, 57H	Writes data to bit devices (X, Y, M, etc.) in units of points.	160 points	o	o	x
	Word units	QW	51H, 57H	Writes data to bit devices (X, Y, M, etc.) in units of 16 points.	10 words (160 points)			
				Writes data to word devices (D, R, T, C, etc.) in units of points.	64 points			
Test (Random Write)	Bit units	JT	4AH, 54H	Sets/resets bit devices (X, Y, M, etc.) in units of points by designating the devices and device numbers at random.	20 points	o	o	x
	Word units	QT	51H, 54H	Sets/resets bit devices (X, Y, M, etc.) in units of 16 points by designating the devices and device numbers at random.	10 words (160 points)			
				Writes data to word devices (D, R, T, C, etc.) in units of points by designating the devices and device numbers at random.	10 points			
Monitor Data Registration	Bit units	JM	4AH, 4DH	Sets the bit devices (X, Y, M, etc.) to be monitored in units of points.	40 points	o	o	o
	Word units	QM	51H, 4DH	Sets the bit devices (X, Y, M, etc.) to be monitored in units of 16 points.	20 words (320 points)			
				Sets the word devices (D, R, T, C, etc.) to be monitored in units of points.	20 points			
Monitor	Bit units	MJ	4DH, 4AH	Monitors the devices registered for monitoring.	—	o	o	o
	Word units	MQ	4DH, 51H					

Note : o .....Executable
x.....Not executable

(b) Device ranges when AnACPU dedicated commands are used

The devices and device number ranges that can be used for device memory access operation are described below.

The device designation code consists of 7 characters.

Leading zeros in the device number (underlined zeros in X000070, for example) can be expressed with a blank code (20H).

Device	+	Device number	=7 characters
{ 1 character (2 characters for T/C) }		{ 6 characters (5 characters for T/C) }	

Bit Device			Word Device		
Device	Device Number Range (Characters)	Decimal/ Hexadecimal Expression	Device	Device Number Range (Characters)	Decimal/ Hexadecimal Expression
Input X	X000000 to X0007FF	Hexadecimal	Timer (present value) T	TN00000 to TN02047	Decimal
Output Y	Y000000 to Y0007FF	Hexadecimal	Counter (present value) C	CN00000 to CN01023	Decimal
Internal relay M	M000000 to M008191	Decimal	Data register D	D000000 to D006143	Decimal
Latch relay L	L000000 to L008191	Decimal	Link register W	W000000 to W000FFF	Hexadecimal
Step relay S	S000000 to S008191	Decimal	File register R	R000000 to R008191	Decimal
Link relay B	B000000 to B000FFF	Hexadecimal	Special register D	D009000 to D009255	Decimal
Annunciator F	F000000 to F002047	Decimal			
Special relay M	M009000 to M009255				
Timer (contact) T	TS00000 to TS02047				
Timer (coil) T	TC00000 to TC02047				
Counter (contact) C	CS00000 to CS01023				
Counter (coil) C	CC00000 to CC01023				

POINTS

(1) To designate the bit device ranges in units of words, the bit device number must be a multiple of 16.

For special relays M, whose device number is M9000 or greater, designation is possible by using "9000 + multiples of 16".

(2) Although the ranges are designated for M, L, and S, if the range for M is designated by L or S, the same processing occurs. This is also true for the ranges for L and S.

(3) The ranges of special relays (M9000 to M9255) and special registers (D9000 to D9255) are divided into the areas for read only, write only, and system use.

Trying to write data to the ranges outside the write-only area might cause the PC CPU to malfunction.

The ACPU programming manual gives details concerning special relays and special registers.

(4) When using an extension file register to read/write file register data from/to a PC CPU, use the commands explained in Section 8.8 for file register (R) read/write operations, use the commands explained in Section 8.8 for read and write operations for the file register (R).

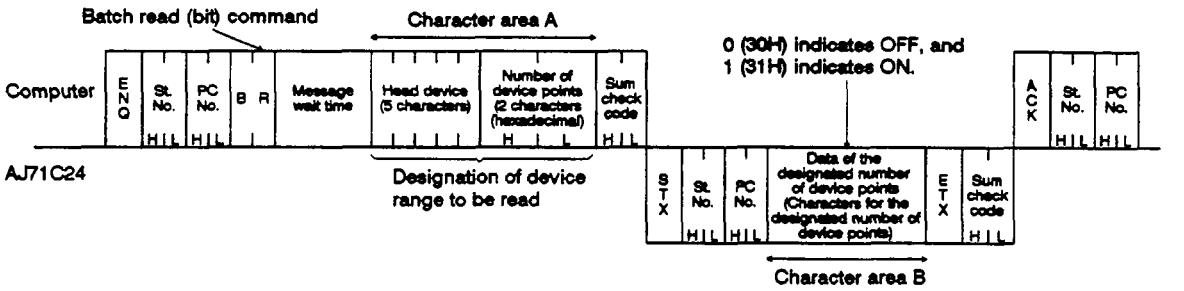
8.7.2 Batch read in units of bits

(a) Using the BR command (ACPU common commands)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



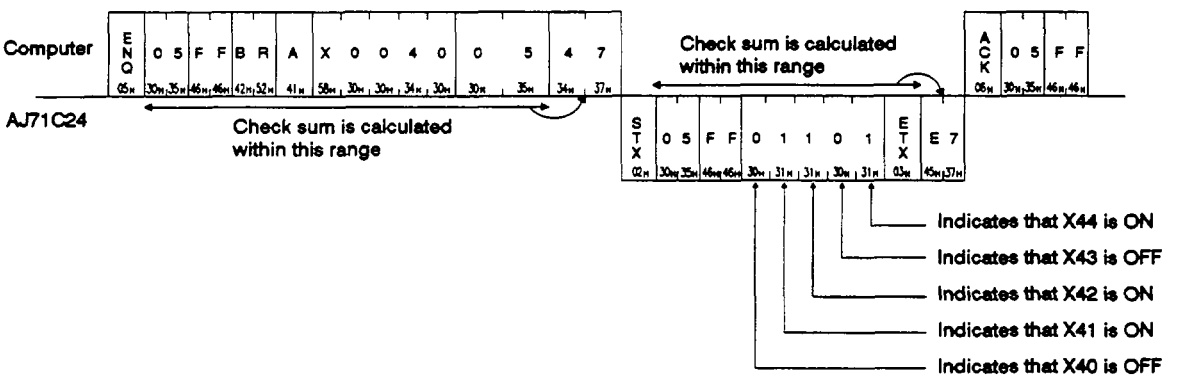
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 256 (setting for 256 points is 00H)
- (Head device number) + [(number of device points) – 1] ≤ maximum device number

Designation Example

To read the data at 5 points from X40 to X44 in station "5". (Message wait time is 100 msec.) (Assume that X40 and X43 are OFF and X41, X42, and X44 are ON.)


Computer
ENQ 0 5 F F B R A X 0 0 4 0 0 5 4 7
Check sum is calculated within this range
ACK 0 5 F F
AJ71C24
Check sum is calculated within this range
STX 0 5 F F 0 1 1 0 1 ETX E 7
Indicates that X44 is ON
Indicates that X43 is OFF
Indicates that X42 is ON
Indicates that X41 is ON
Indicates that X40 is OFF

POINT

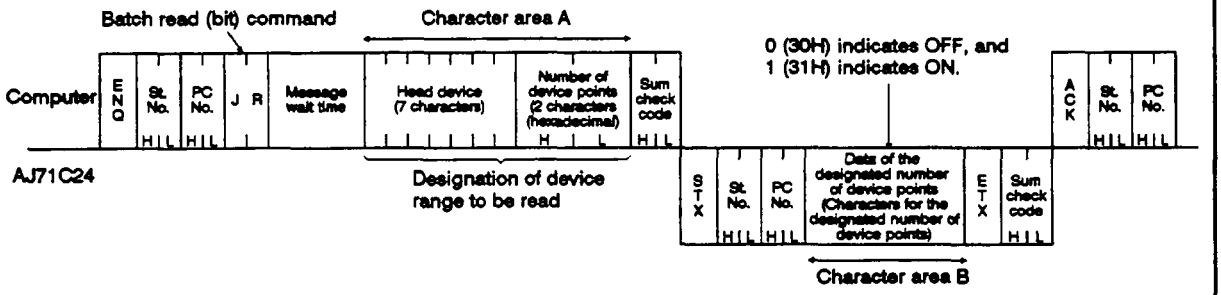
The message wait time is designated in the range of 0 to 150 msec in units of 10 msec, using hexadecimal notation of 0 through FH. Therefore, 100 msec corresponds to "A".

(b) Using the JR command (AnACPU dedicated command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



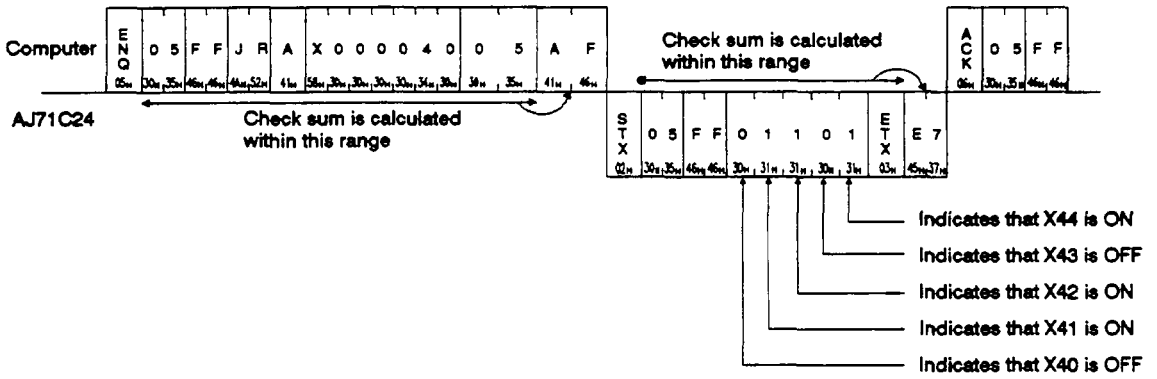
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 256 (setting for 256 points is 00H)
- (Head device number) + [(number of device points) – 1] ≤ maximum device number

Designation Example

To read the data at 5 points from X40 to X44 in station "5". (Message wait time is 100 msec.) (Assume that X40 and X43 are OFF and X41, X42, and X44 are ON.)


Computer
ENQ 0 5 F F J R A X 0 0 0 0 4 0 0 5 A F
Check sum is calculated within this range
ACK 0 5 F F
AJ71C24
Check sum is calculated within this range
STX 0 5 F F 0 1 1 0 1 ETX E 7
Indicates that X44 is ON
Indicates that X43 is OFF
Indicates that X42 is ON
Indicates that X41 is ON
Indicates that X40 is OFF

POINT

The message wait time is designated in the range of 0 to 150 msec in units of 10 msec, using hexadecimal notation of 0 to FH. Therefore, 100 msec corresponds to "A".

8.7.3 Batch read in units of words

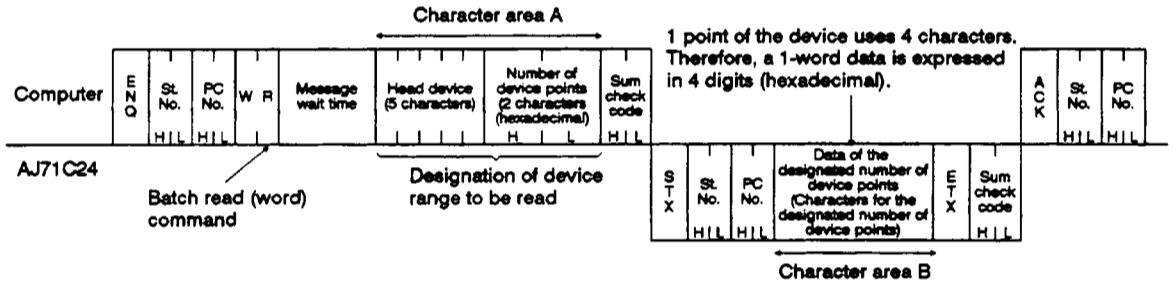
The method for specifying the control protocol and examples are shown below for a batch read of word device memory and batch read of bit device memory (16-point units).

(a) Using the WR command (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.


Character area A
1 point of the device uses 4 characters. Therefore, a 1-word data is expressed in 4 digits (hexadecimal).
Computer
ENQ
St. No.
PC No.
W R
Message wait time
Head device (5 characters)
Number of device points (2 characters (hexadecimal))
Sum check code
ACK
AJ71C24
Batch read (word) command
Designation of device range to be read
STX
ETX
Data of the designated number of device points (Characters for the designated number of device points)
Character area B

POINT

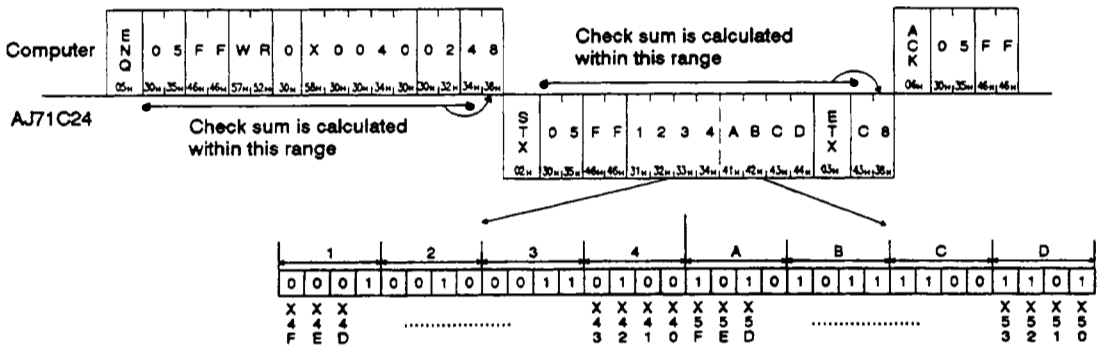
To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 64 (32 for a bit device)
- (Head device number) + [(number of device points**) – 1] ≤ maximum device number

** ("number of device points" x 16 for a bit device)

Designation Examples

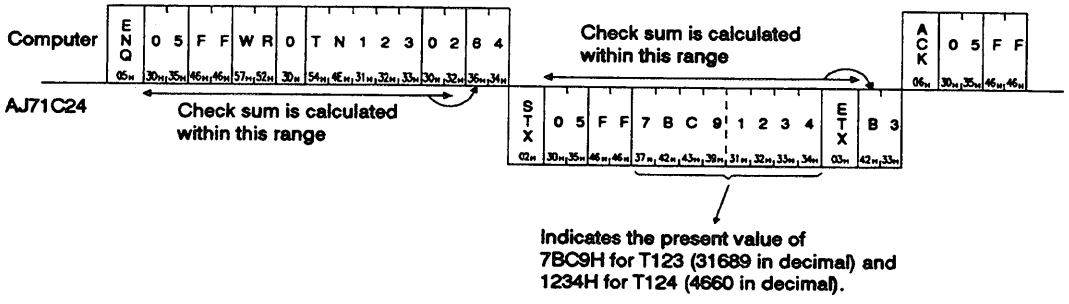
Example 1:
To read data at 32 points from X40 to X5F in station "5".
(Message wait time is 0 msec)


Computer
ENQ 0 5 F F W R 0 X 0 0 4 0 0 2 4 8
Check sum is calculated within this range
ACK 0 5 F F
AJ71C24
Check sum is calculated within this range
STX 0 5 F F 1 2 3 4 A B C D ETX C 8
1 2 3 4 A B C D
0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 1 0 1 0 1 0 1 1 1 1 0 0 1 1 0 1
X X X
4 4 4
F E D
X X X X X X X X
4 4 4 4 5 5 5 5
3 2 1 0 F E D
X X X X
5 5 5 5
3 2 1 0

POINT

The WR command is used for word unit designation. The designation for 32 points of devices from X40 to X5F is "02" ("1" for 16 points).

Example 2:
To read the present values at 2 points of T123 and T124 in station "5".

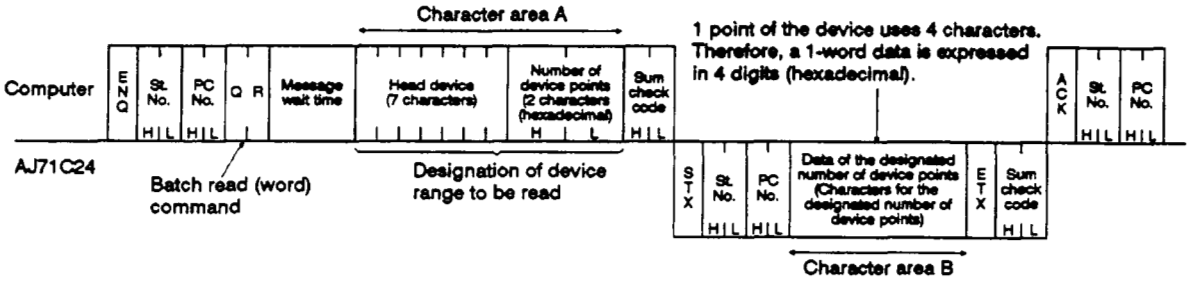

Computer
AJ71C24
ENQ 05H
0 5 F F W R 0 T N 1 2 3 0 2 8 4
Check sum is calculated within this range
Check sum is calculated within this range
ACK 06H
0 5 F F
STX 02H
0 5 F F 7 B C 9 1 2 3 4
ETX 03H
B 3
Indicates the present value of 7BC9H for T123 (31689 in decimal) and 1234H for T124 (4660 in decimal).

(b) Using the QR command (AnACPU dedicated command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.


Character area A
1 point of the device uses 4 characters. Therefore, a 1-word data is expressed in 4 digits (hexadecimal).
Computer
ENQ
St. No.
PC No.
Q R
Message wait time
Head device (7 characters)
Number of device points (2 characters (hexadecimal))
Sum check code
ACK
AJ71C24
Batch read (word) command
Designation of device range to be read
STX
Data of the designated number of device points (Characters for the designated number of device points)
ETX
Character area B

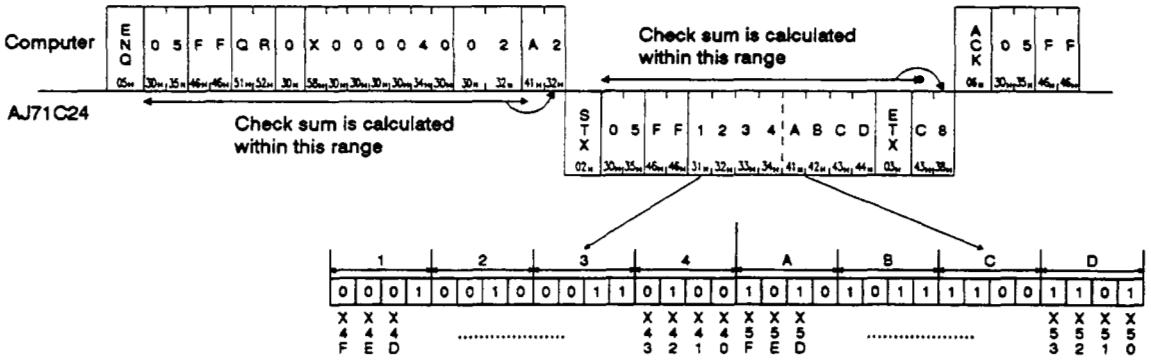
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 64 (32 for a bit device)
- (Head device number) + [(number of device points**) – 1] ≤ maximum device number
  ** ("number of device points" x 16 for a bit device)

Designation Examples

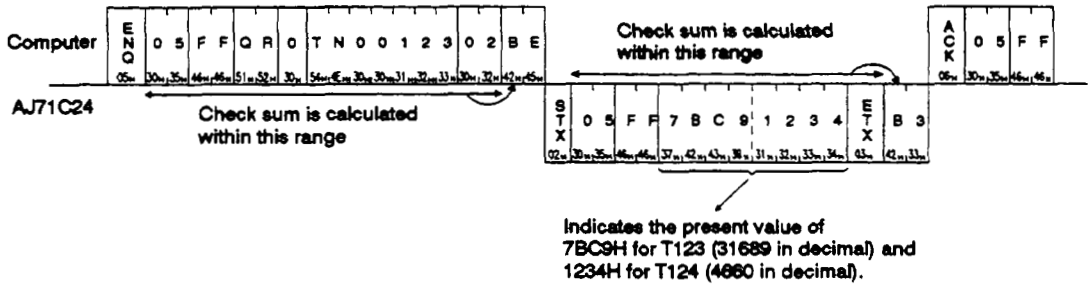
Example 1:
To read data at 32 points from X40 to X5F in station "5".
(Message wait time is 0 msec)


Computer
ENQ 0 5 F F Q R 0 X 0 0 0 0 4 0 0 2 A 2
Check sum is calculated within this range
ACK 0 5 F F
AJ71C24
Check sum is calculated within this range
STX 0 5 F F 1 2 3 4 A B C D ETX C 8
1 2 3 4 A B C D
0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 1 0 1 0 1 0 1 1 1 1 0 0 1 1 0 1
X4FE X4ED X443 X442 X441 X440 X55F X55E X553 X552 X551 X550

POINT

The QR command is used for word unit designation. The designation for 32 points of devices from X40 to X5F is "02" ("1" for 16 points).

Example 2:
To read the present values at 2 points of T123 and T124 in station "5".


Computer
AJ71C24
ENQ 0 5 F F Q R 0 T N 0 0 1 2 3 0 2 B E
Check sum is calculated within this range
Check sum is calculated within this range
ACK 0 5 F F
STX 0 5 F F 7 B C 9 1 2 3 4 ETX B 3
Indicates the present value of 7BC9H for T123 (31689 in decimal) and 1234H for T124 (4660 in decimal).

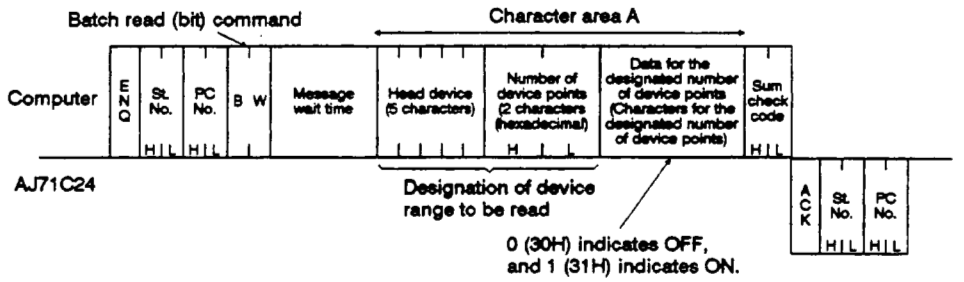
8.7.4 Batch write in units of bits

(a) Using the BW command (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



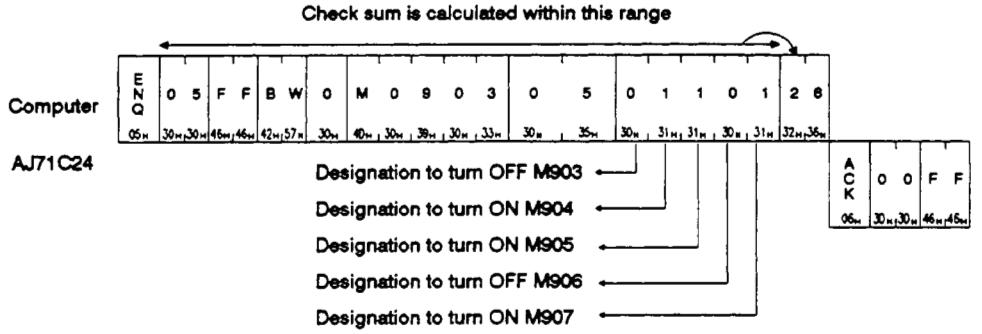
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 160
- (Head device number) + [(number of device points) − 1] ≤ maximum device number

Designation Example

To write data to 5 points from M903 to M907 in station "0".
(Message wait time is 0 msec)

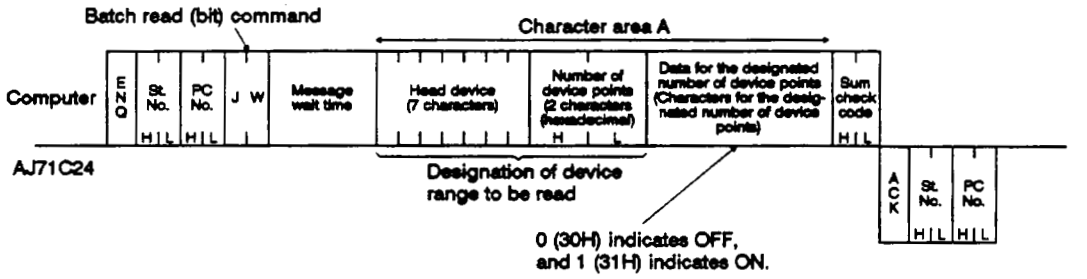

Check sum is calculated within this range
Computer
AJ71C24
ENQ 05H
0 5 30H 35H
F F 46H 46H
B W 42H 57H
0 30H
M 0 9 0 3 4DH 30H 39H 30H 33H
0 5 30H 35H
0 1 1 0 1 30H 31H 31H 30H 31H
2 6 32H 36H
Designation to turn OFF M903
Designation to turn ON M904
Designation to turn ON M905
Designation to turn OFF M906
Designation to turn ON M907
ACK 06H
0 0 30H 30H
F F 46H 46H

(b) Using the JW command (AnACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



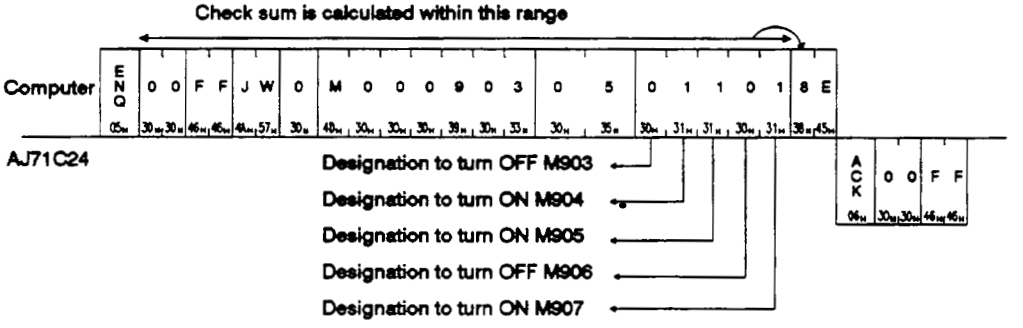
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 160
- (Head device number) + [(number of device points) – 1] ≤ maximum device number

Designation Example

To write data to 5 points from M903 to M907 in station "0".
(Message wait time is 0 msec)


Check sum is calculated within this range
Computer
ENQ 0 0 F F J W 0 M 0 0 0 9 0 3 0 5 0 1 1 0 1 8 E
AJ71C24
Designation to turn OFF M903
Designation to turn ON M904
Designation to turn ON M905
Designation to turn OFF M906
Designation to turn ON M907
ACK 0 0 F F

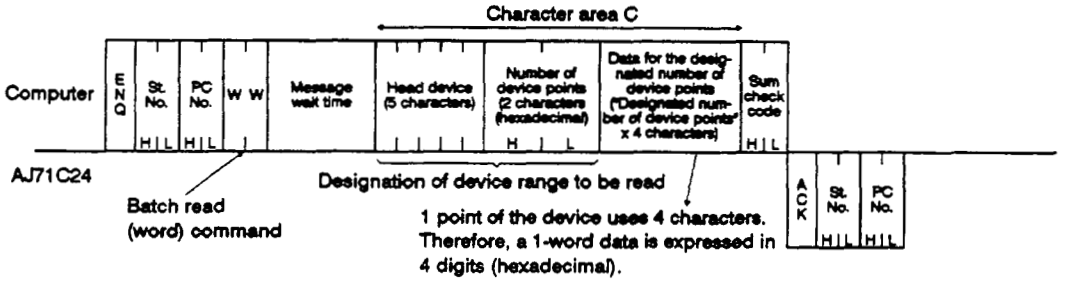
8.7.5 Batch write in units of words

(a) Using the WW command (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.


Character area C
Computer
ENQ
St. No.
PC No.
W W
Message wait time
Head device (5 characters)
Number of device points (2 characters (hexadecimal))
Data for the designated number of device points ("Designated number of device points" x 4 characters)
Sum check code
H L
AJ71C24
Batch read (word) command
Designation of device range to be read
1 point of the device uses 4 characters. Therefore, a 1-word data is expressed in 4 digits (hexadecimal).
ACK
St. No.
PC No.

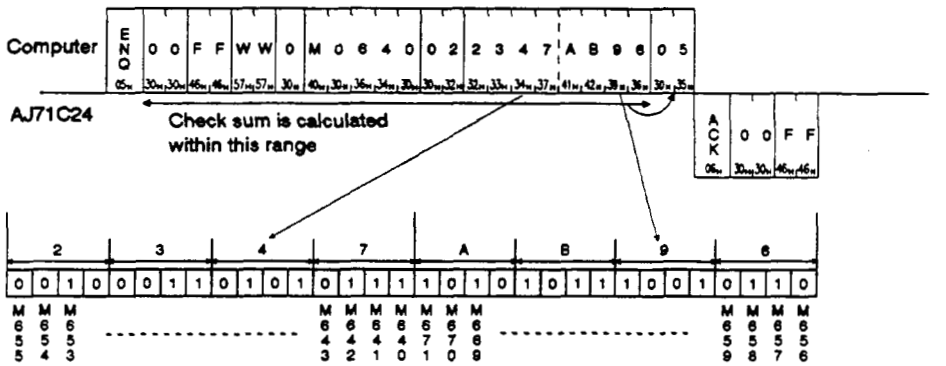
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 64 (10 for a bit device)
- (Head device number) + [(number of device points**) – 1] ≤ maximum device number
  **("number of device points" x 16 for a bit device)

Designation Examples

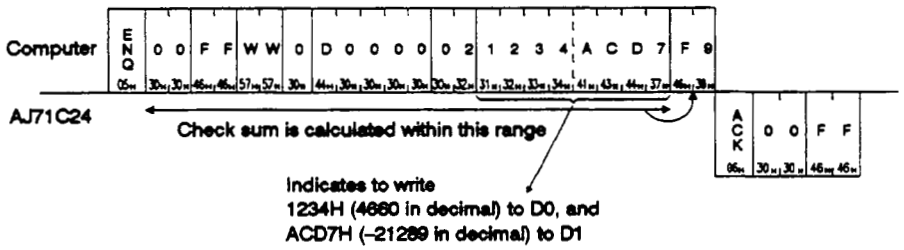
Example 1:
To write data to 32 points from M640 to M671 in station "0".
(Message wait time is 0 msec)



POINT

The WW command is used for word unit designation. The designation for the number of device point to write data to the 32 points to M640 to M671 is "02" ("1" for 16 points).

Example 2: To write data tc 2 points of D0 and D1 in station "0".
(Message wait time: 0 mesc)

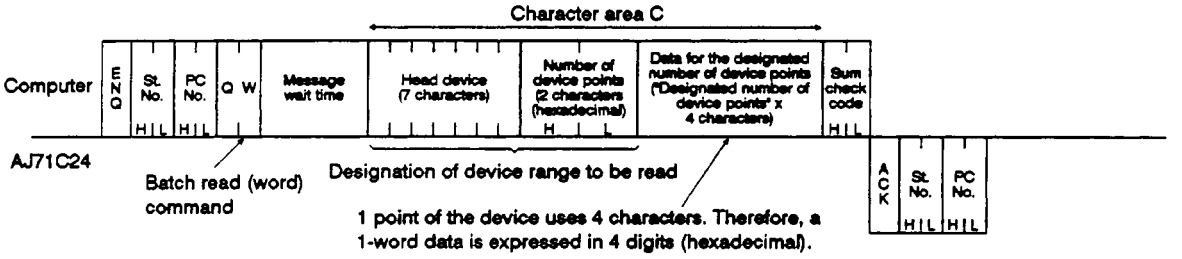

Computer
ENQ 0 0 F F W W 0 D 0 0 0 0 0 2 1 2 3 4 A C D 7 F 9
AJ71C24
Check sum is calculated within this range
ACK 0 0 F F
Indicates to write
1234H (4660 in decimal) to D0, and
ACD7H (–21289 in decimal) to D1

(b) Using the QW command (AnACPU dedicated command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.


Character area C
Computer
ENQ
St. No.
PC No.
Q W
Message wait time
Head device (7 characters)
Number of device points (2 characters (hexadecimal))
Data for the designated number of device points ("Designated number of device points" x 4 characters)
Sum check code
H L
AJ71C24
Batch read (word) command
Designation of device range to be read
1 point of the device uses 4 characters. Therefore, a 1-word data is expressed in 4 digits (hexadecimal).
ACK
St. No.
PC No.

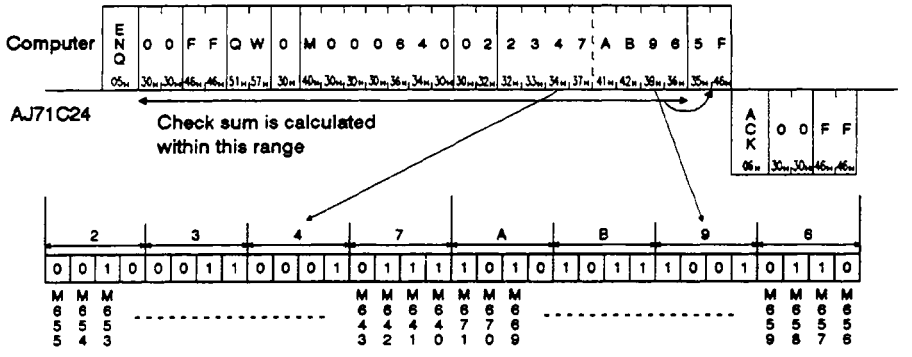
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 64 (10 for a bit device)
- (Head device number) + [(number of device points**) – 1] ≤ maximum device number
  **("number of device points" x 16 for a bit device)

Designation Examples

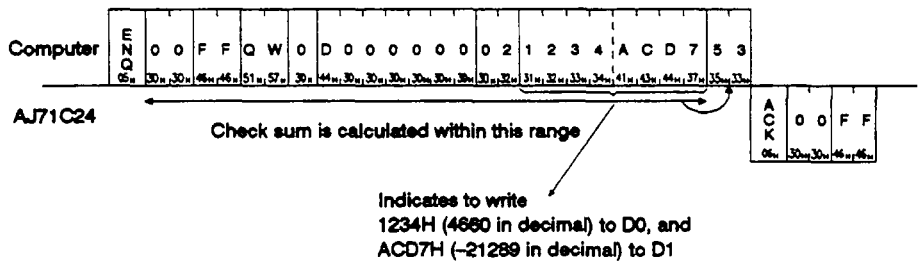
Example 1:
To write data to 32 points from M640 to M671 in station "0".
(Message wait time is 0 msec)



POINT

The QW command is used for word unit designation. The designation for the number of device point to write data to 32 points from M640 to M671 is "02" ("1" for 16 points).

Example 2: To write data to 2 points of D0 and D1 in station "0".
(Message wait time: 0 mesc)


Computer
AJ71C24
ENQ
0 0 F F Q W 0 D 0 0 0 0 0 0 0 2 1 2 3 4 A C D 7 5 3
ACK
0 0 F F
Check sum is calculated within this range
Indicates to write
1234H (4660 in decimal) to D0, and
ACD7H (–21289 in decimal) to D1

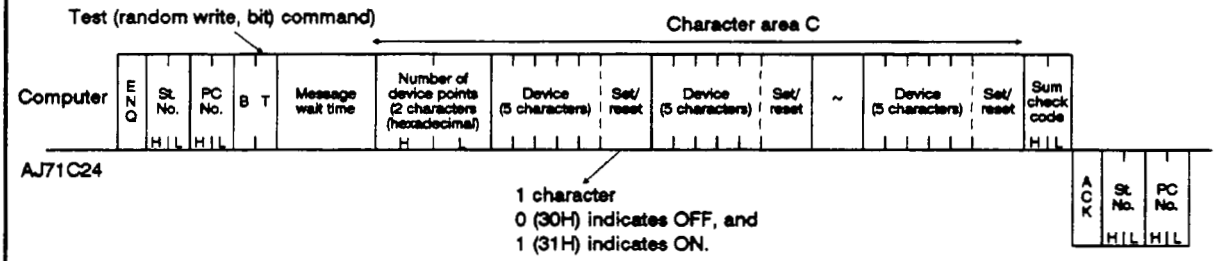
8.7.6 Testing device memory in units of bit (random write)

(a) Using the BT command (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



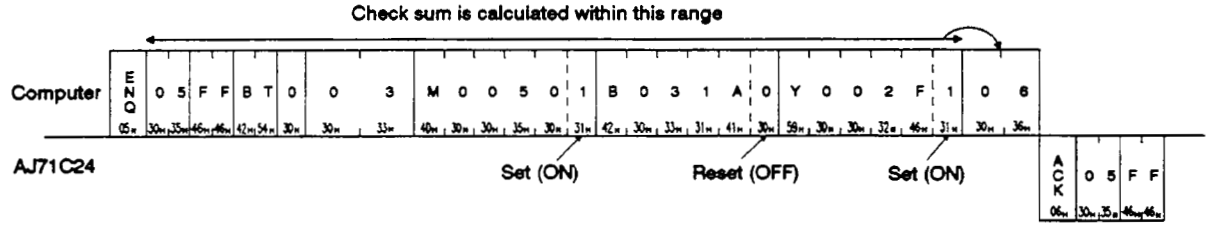
POINT

To designate the device range, the following condition must be met:

- 1 ≤ number of device points ≤ 20

Designation Example

To write ON to M50, OFF to B31A, and ON to Y2F in station "5".
(Message wait time is 0 msec)

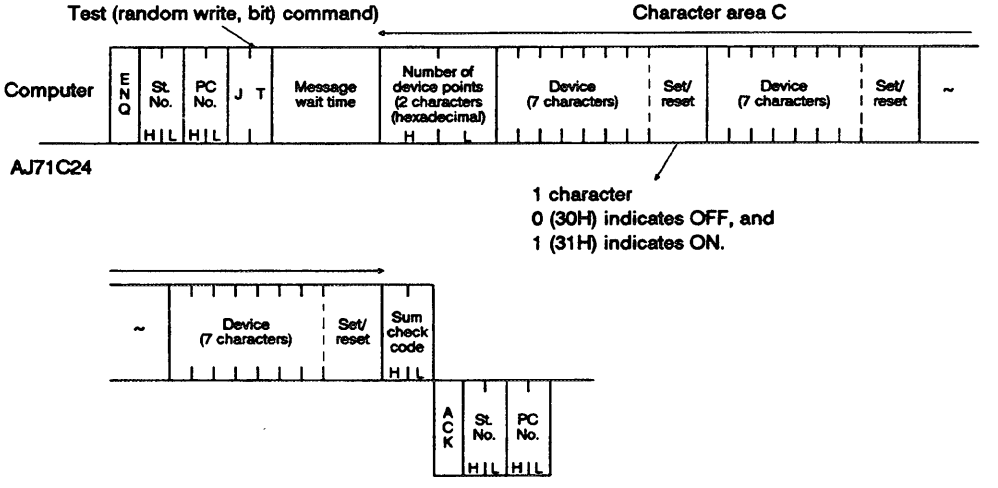

Check sum is calculated within this range
Computer
ENQ
0 5 F F B T 0 0 3 M 0 0 5 0 1 B 0 3 1 A 0 Y 0 0 2 F 1 0 6
AJ71C24
Set (ON)
Reset (OFF)
Set (ON)
ACK
0 5 F F

(b) Using the JT command (AnACPU dedicated command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



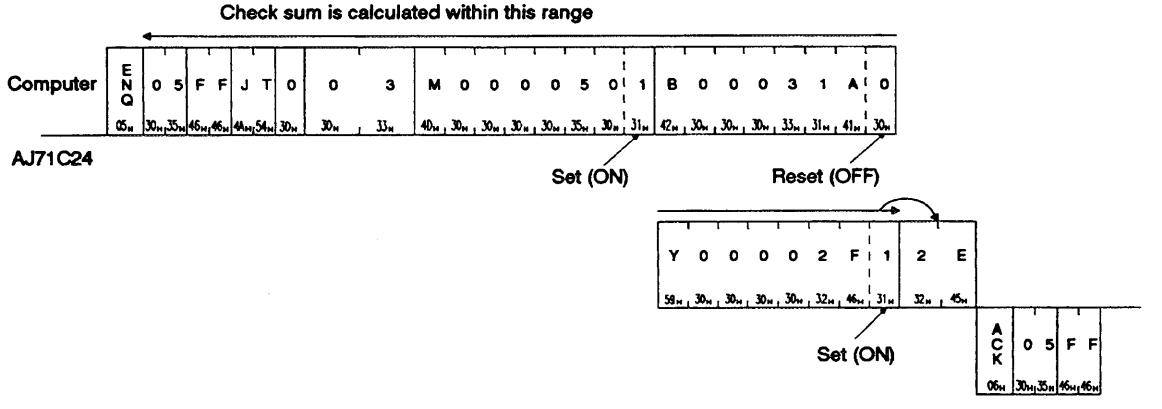
POINT

To designate the device range, the following condition must be met:

- 1 ≤ number of device points ≤ 20

Designation Example

To write ON to M50, OFF to B31A, and ON to Y2F in station "5".
(Message wait time is 0 msec)


Check sum is calculated within this range
Computer
ENQ 0 5 F F J T 0 0 3 M 0 0 0 0 5 0 1 B 0 0 0 3 1 A 0
AJ71C24
Set (ON)
Reset (OFF)
Y 0 0 0 0 2 F 1 2 E
Set (ON)
ACK 0 5 F F

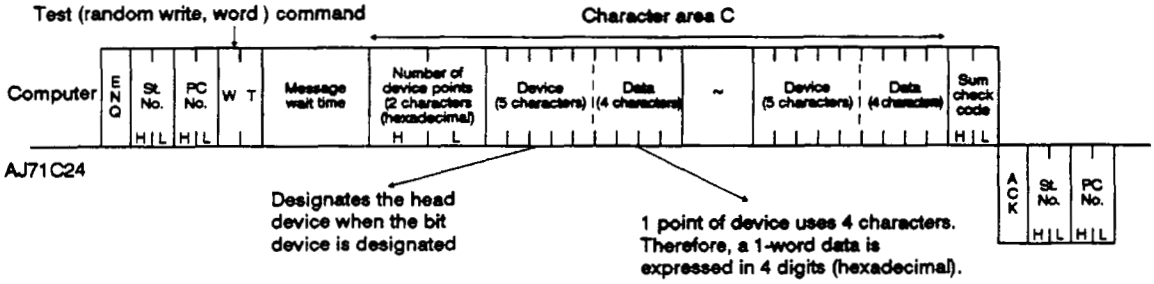
8.7.7 Testing device memory in units of words (random write)

(a) Using the WT command (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



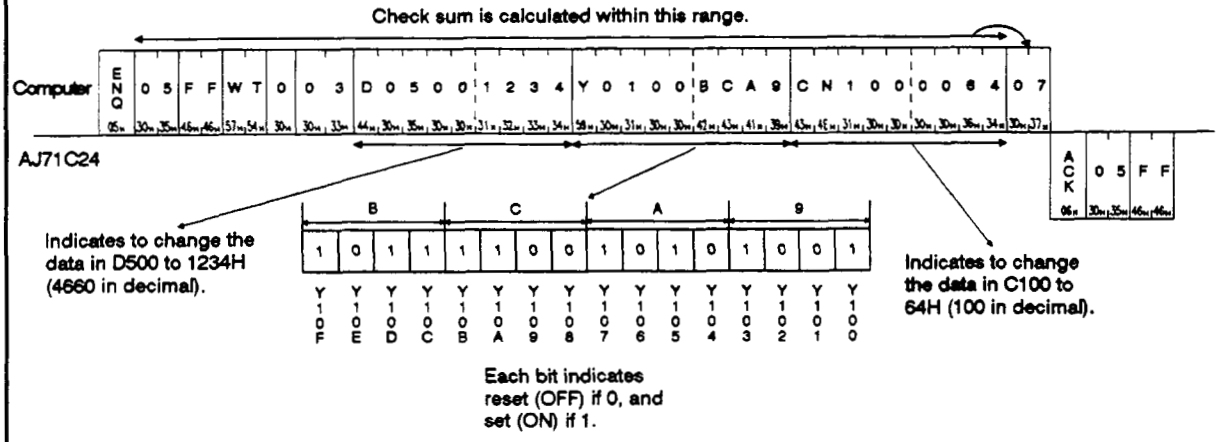
POINT

To designate the device range, the following condition must be met:

- 1 ≤ number of device points ≤ 10 (10 units for bit devices where 1 unit corresponds to 16 points)

Designation Example

To change the present value in station number "5" as indicated below.
(Message wait time is 0 msec)

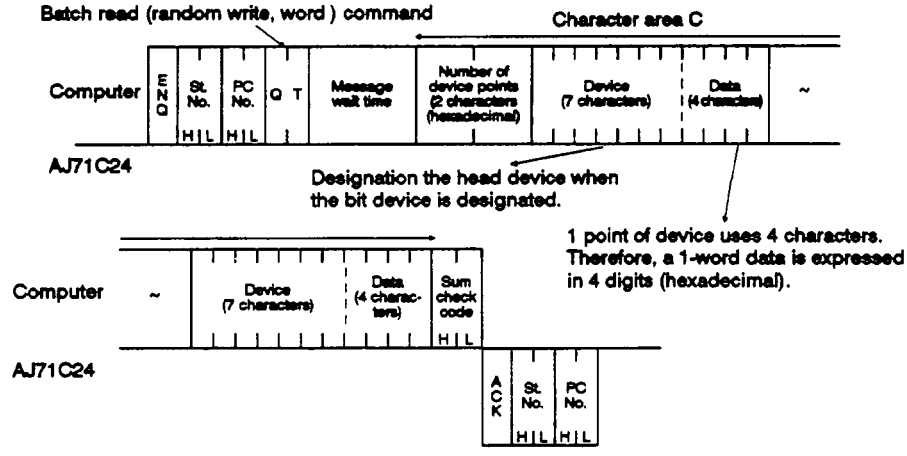

Check sum is calculated within this range.
Computer
ENQ 0 5 F F W T 0 0 3 D 0 5 0 0 1 2 3 4 Y 0 1 0 0 B C A 9 C N 1 0 0 0 0 6 4 0 7
AJ71C24
ACK 0 5 F F
Indicates to change the data in D500 to 1234H (4660 in decimal).
B C A 9
1 0 1 1 1 1 0 0 1 0 1 0 1 0 0 1
Y 1 0 F Y 1 0 E Y 1 0 D Y 1 0 C Y 1 0 B Y 1 0 A Y 1 0 9 Y 1 0 8 Y 1 0 7 Y 1 0 6 Y 1 0 5 Y 1 0 4 Y 1 0 3 Y 1 0 2 Y 1 0 1 Y 1 0 0
Indicates to change the data in C100 to 64H (100 in decimal).
Each bit indicates reset (OFF) if 0, and set (ON) if 1.

(b) Using the QT command (AnACPU dedicated command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



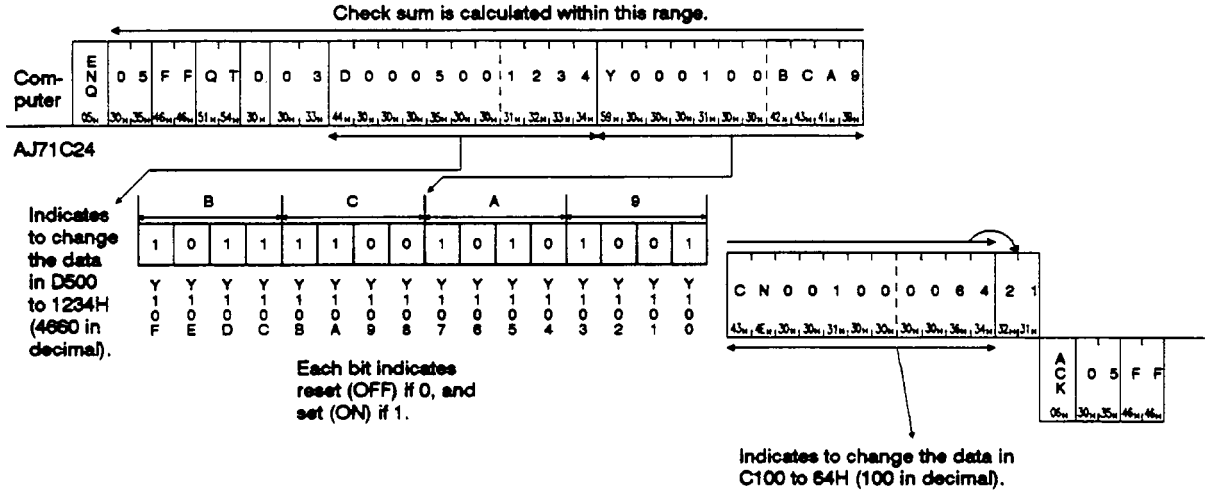
POINT

To designate the device range, the following condition must be met:

- 1 ≤ number of device points ≤ 10 (10 units for bit devices where 1 unit corresponds to 16 points)

Designation Example

To change the present value in station number "5" as indicated below.
(Message wait time is 0 msec)

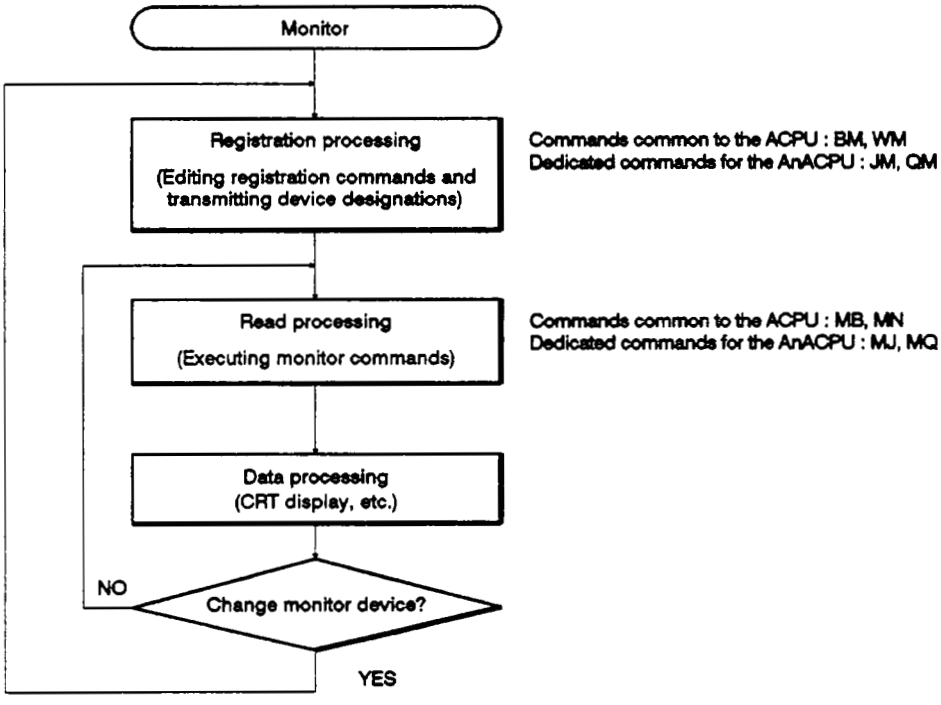

Check sum is calculated within this range.
Com-puter
ENQ 0 5 F F Q T 0 0 3 D 0 0 0 5 0 0 1 2 3 4 Y 0 0 0 1 0 0 B C A 9
AJ71C24
Indicates to change the data in D500 to 1234H (4660 in decimal).
B C A 9
1 0 1 1 1 1 0 0 1 0 1 0 1 0 0 1
Y F E D C B A 9 8 7 6 5 4 3 2 1 0
Each bit indicates reset (OFF) if 0, and set (ON) if 1.
C N 0 0 1 0 0 0 0 6 4 2 1
ACK 0 5 F F
Indicates to change the data in C100 to 64H (100 in decimal).

8.7.8 Monitoring device memory

Monitor data registration is the function that registers the name and the number of the device to be monitored by the computer to the AJ71C24. The monitor is the function that (a) reads the data content of the device registered at the time the monitor read command is executed by the computer, and (b) executes the corresponding processing such as monitoring.

The device numbers must be consecutive when the device is read using the batch read (BR, WR/JR, QR) command. However, when this function is used, it is possible to read and monitor the devices by designating the device numbers at random.

(1) Control procedure for monitoring


Monitor
Registration processing
(Editing registration commands and transmitting device designations)
Commands common to the ACPU : BM, WM
Dedicated commands for the AnACPU : JM, QM
Read processing
(Executing monitor commands)
Commands common to the ACPU : MB, MN
Dedicated commands for the AnACPU : MJ, MQ
Data processing
(CRT display, etc.)
NO
Change monitor device?
YES

POINTS

(1) As the flowchart shows, monitor data registration must be executed before monitoring. Attempting to execute monitoring without registering the monitor data will cause a protocol error.

(2) The contents of the monitor data registration area are cleared when the power supply is turned OFF, the PC CPU is reset, or the mode is switched.

(3) For monitor registration, five types of registration are possible. They are device memory in bit units (BM or JM), device memory in word units (WM or QM), and the extension file register (EM).

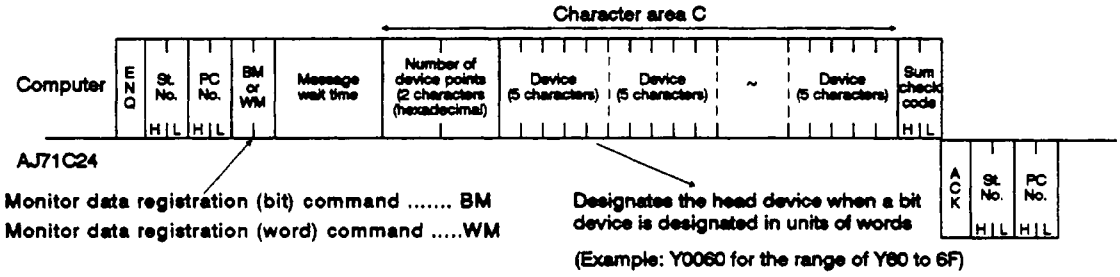
(2) Registering monitor data of device memory

(a) Using the BM or WM command (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



POINTS

(1) To designate the device range, the following conditions must be met:

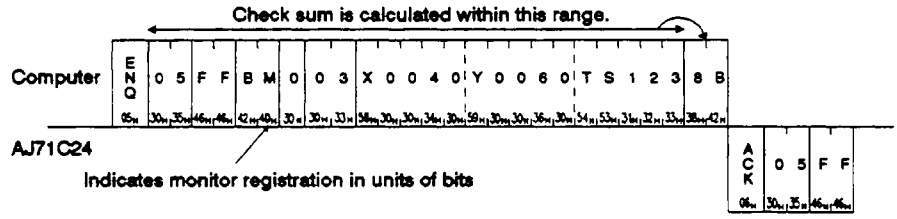
With PC CPUs other than A3HCPU, A2ACPU(S1), and A3ACPU, 1 point of device X (input) is counted as 2 points for processing.

- BM command 1 ≤ number of device points ≤ 40
- WM command 1 ≤ number of device points ≤ 20

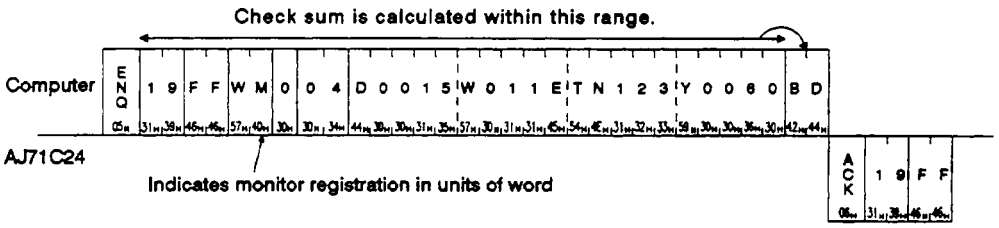
(2) With the WM command, word devices and bit devices (16 point units) can be used in combination, as shown in Example 2.

Designation Examples

Example 1:
To display monitor registration for X40, Y60, and T123 (contact) in station number "5".
(Message wait time is 0 msec)


Check sum is calculated within this range.
Computer
ENQ
0 5 F F B M 0 0 3 X 0 0 4 0 Y 0 0 6 0 T S 1 2 3 8 B
AJ71C24
ACK
0 5 F F
Indicates monitor registration in units of bits

Example 2 :
To register monitor data for D15, W11E, T123 (present value), and Y60 to Y6F in station number "25". (Message wait time is 0 msec)


Check sum is calculated within this range.
Computer
ENQ 1 9 F F W M 0 0 4 D 0 0 1 5 W 0 1 1 E T N 1 2 3 Y 0 0 6 0 B D
AJ71C24
Indicates monitor registration in units of word
ACK 1 9 F F

POINT

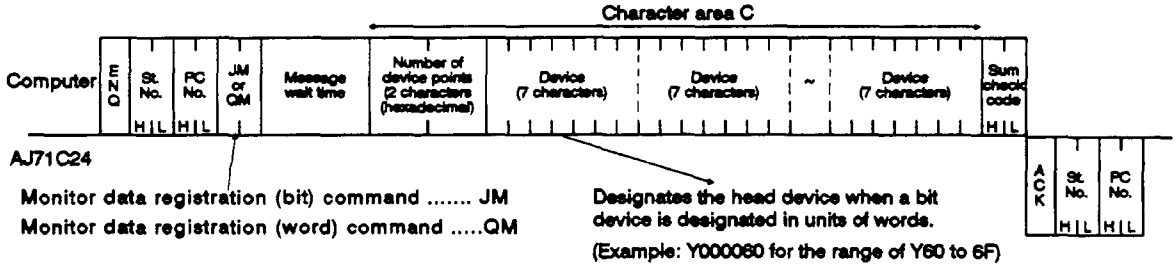
The station number is designated in hexadecimal. Therefore, the designation of station number "25" should be made in 19H.

(b) Using the JM or QM commands (AnACPU dedicated commands)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



POINTS

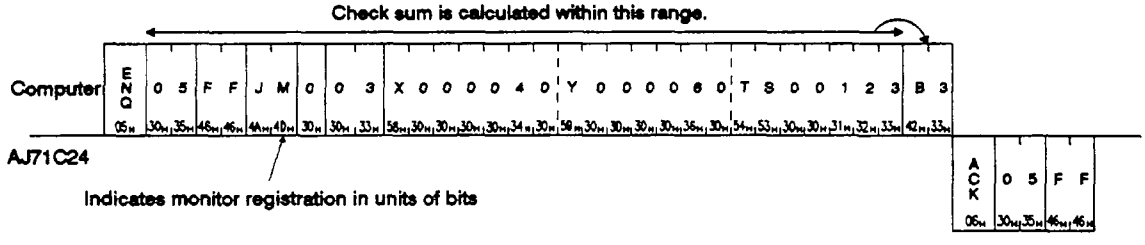
(1) To designate the device range, the following conditions must be met:

- JM command 1 ≤ number of device points ≤ 40
- QM command 1 ≤ number of device points ≤ 20

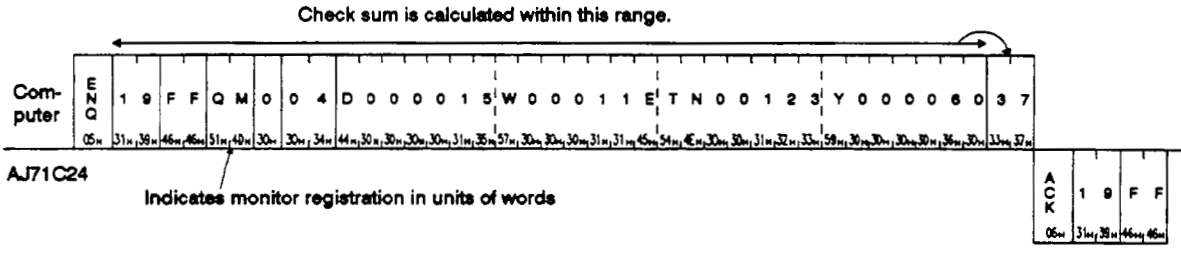
(2) With the QM command, word devices and bit devices (16-point units) can be used in combination as shown in Example 2.

Designation Examples

Example 1:
To register monitor data for X40, Y60, and T123 (contact) in station number "5".
(Message wait time is 0 msec)


Check sum is calculated within this range.
Computer
ENQ 0 5 F F J M 0 0 3 X 0 0 0 0 4 0 Y 0 0 0 0 6 0 T S 0 0 1 2 3 B 3
AJ71C24
ACK 0 5 F F
Indicates monitor registration in units of bits

Example 2:
To register monitor data for D15, W11E, T123 (present value), and Y60 to Y6F in station number 25. (Message wait time is 0 msec)


Check sum is calculated within this range.
Com-puter
ENQ
1 9 F F Q M 0 0 4 D 0 0 0 0 1 5 W 0 0 1 1 E T N 0 0 1 2 3 Y 0 0 0 0 6 0 3 7
AJ71C24
Indicates monitor registration in units of words
ACK
1 9 F F

POINT

The station number is designated in hexadecimal. Therefore, the designation of station number 25 should be made in 19H.

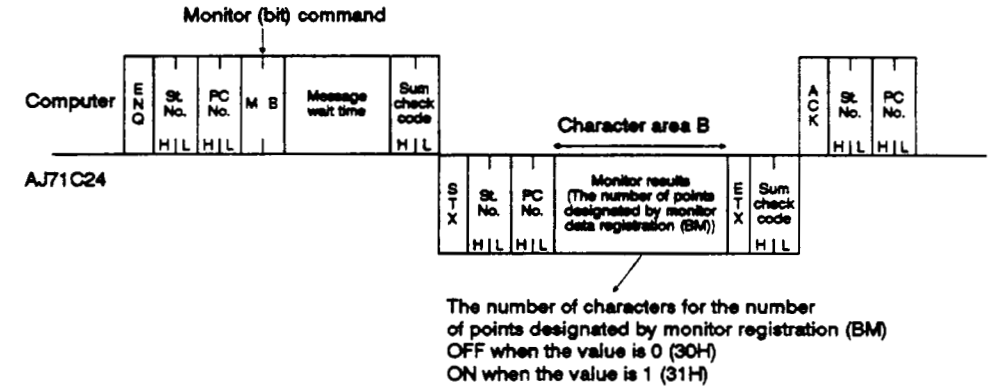
(3) Monitoring device memory in units of bits

(a) Monitoring the devices registered by the BM command (ACPU common command)

Designation Method

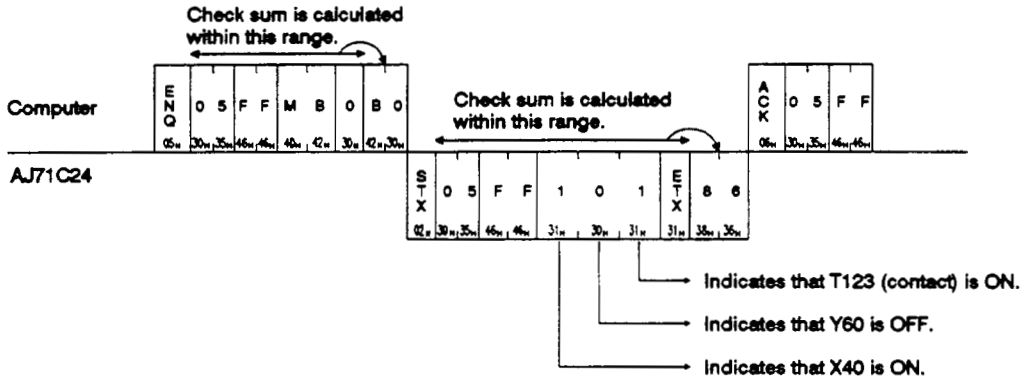
St. No. : Station number

Designation in protocol 1 is shown below.



Designation Example

Monitoring is executed after registering the monitor data (bit units) in Example 1 of (2) (a) (Message wait time is 0 msec)

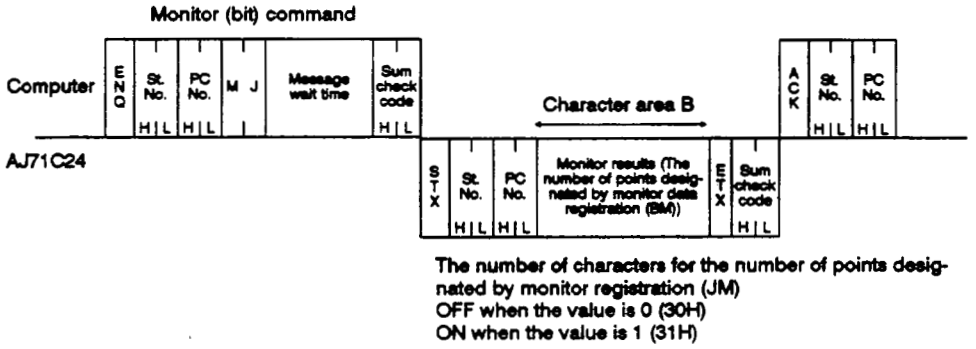

Check sum is calculated within this range.
Computer
ENQ 0 5 F F M B 0 B 0
Check sum is calculated within this range.
ACK 0 5 F F
AJ71C24
STX 0 5 F F 1 0 1 ETX 8 6
Indicates that T123 (contact) is ON.
Indicates that Y60 is OFF.
Indicates that X40 is ON.

(b) Monitoring the devices registered by the JM command (AnACPU dedicated command)

Designation Method

St. No. : Station number

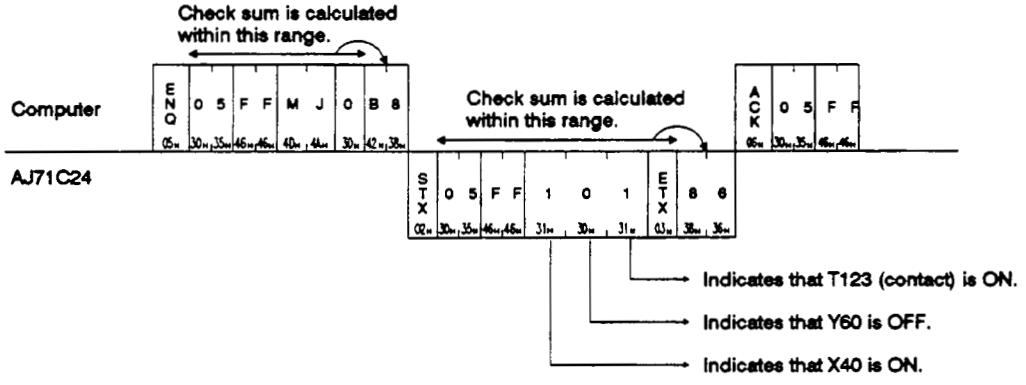
Designation in protocol 1 is shown below.



The number of characters for the number of points designated by monitor registration (JM)
OFF when the value is 0 (30H)
ON when the value is 1 (31H)

Designation Example

Monitoring is executed after registering the monitor data (bit units) in Example 1 of (2) (b) (Message wait time is 0 msec)


Check sum is calculated within this range.
Computer
ENQ 0 5 F F M J 0 B 8
Check sum is calculated within this range.
ACK 0 5 F F
AJ71C24
STX 0 5 F F 1 0 1 ETX 8 6
Indicates that T123 (contact) is ON.
Indicates that Y60 is OFF.
Indicates that X40 is ON.

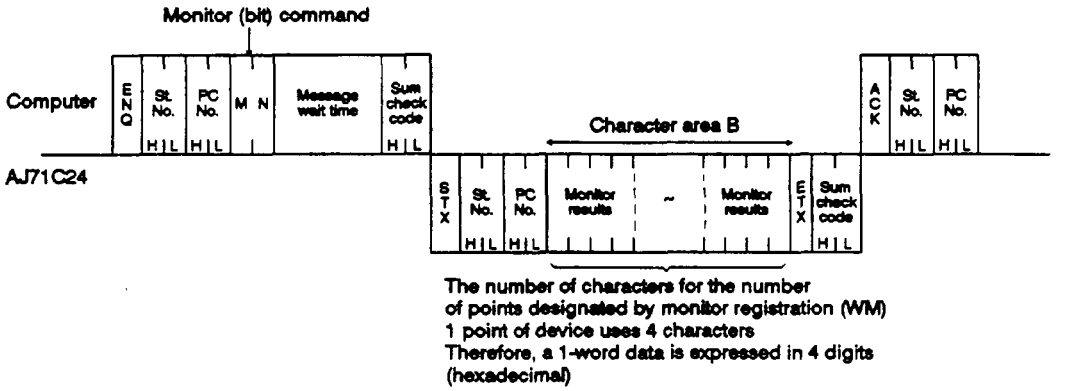
(4) Monitoring device memory in units of words

(a) Monitoring the device registered by the WM command (ACPU common command)

Designation Method

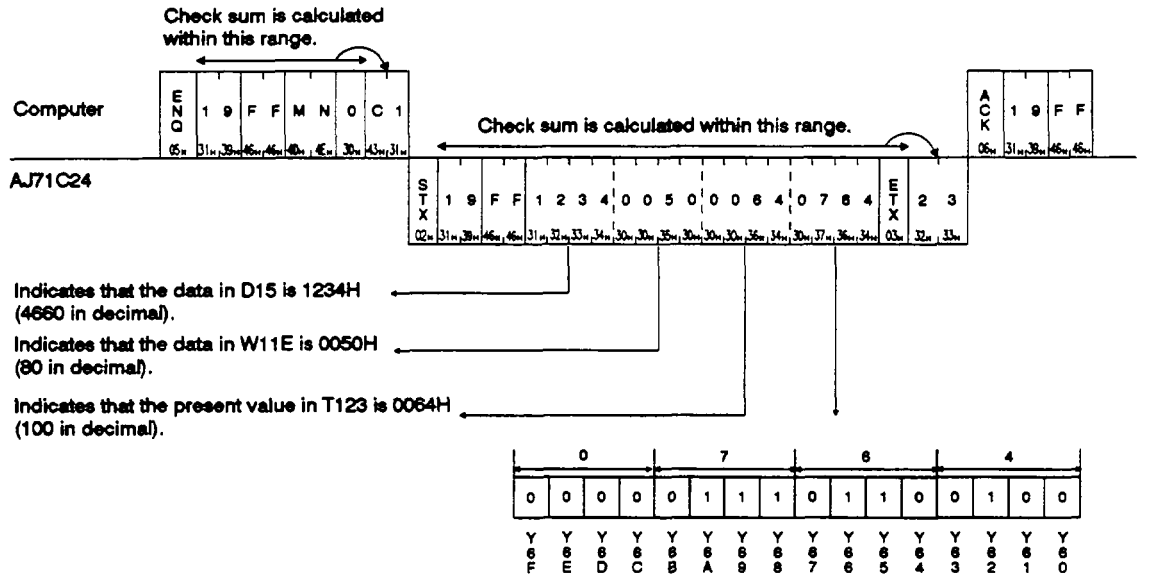
St. No. : Station number

Designation in protocol 1 is shown below.



Designation Example

Monitoring is executed after registering the monitor data (word units) as in Example 2 of (2) (a) (Message wait time is 0 msec)

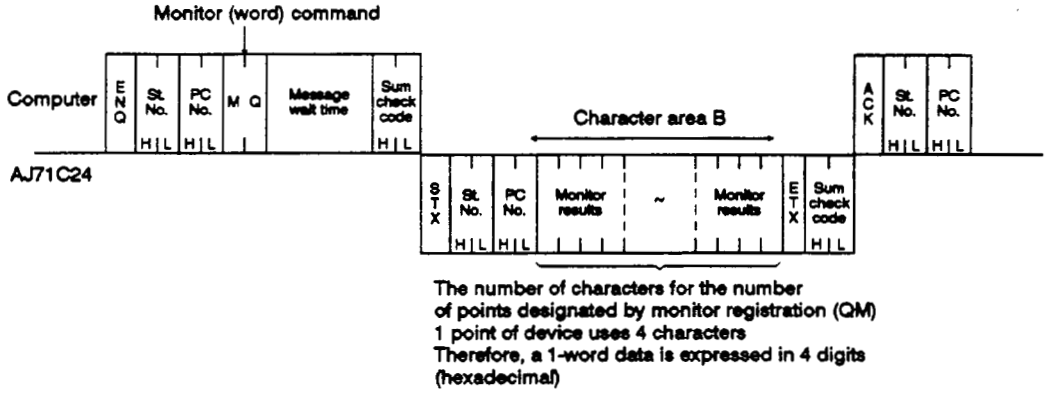

Check sum is calculated within this range.
Computer
ENQ 1 9 F F M N 0 C 1
Check sum is calculated within this range.
ACK 1 9 F F
AJ71C24
STX 1 9 F F 1 2 3 4 0 0 5 0 0 0 6 4 0 7 8 4 ETX 2 3
Indicates that the data in D15 is 1234H (4660 in decimal).
Indicates that the data in W11E is 0050H (80 in decimal).
Indicates that the present value in T123 is 0064H (100 in decimal).
0 7 6 4
0 0 0 0 0 1 1 1 0 1 1 0 0 1 0 0
Y6F Y6E Y6D Y6C Y6B Y6A Y69 Y68 Y67 Y66 Y65 Y64 Y63 Y62 Y61 Y60

(b) Monitoring the devices registered by the QM command (AnACPU dedicated command)

Designation Method

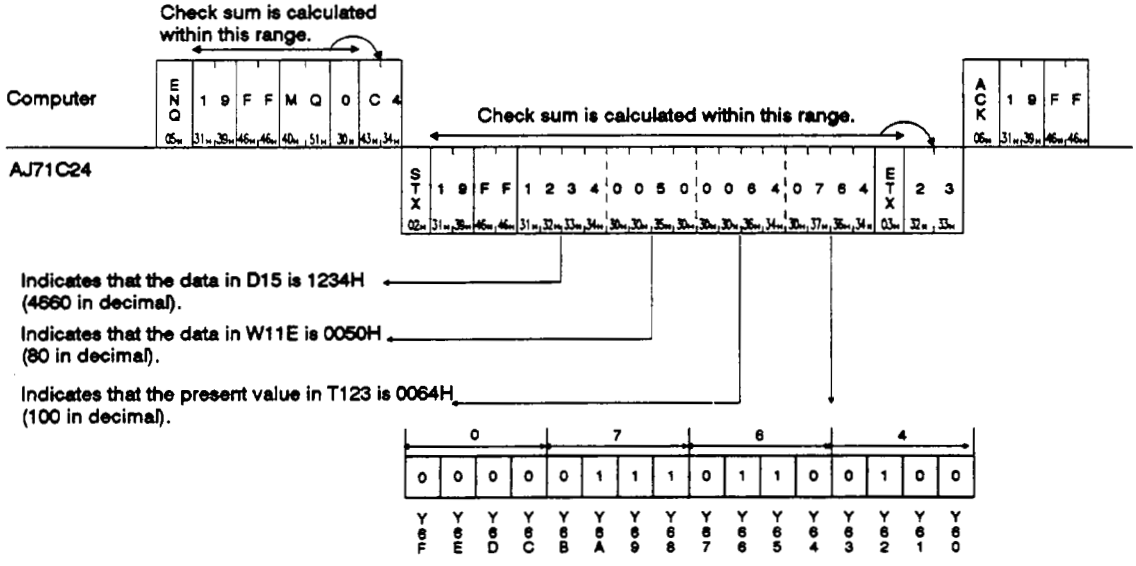
St. No. : Station number

Designation in protocol 1 is shown below.



Designation Example

Monitoring is executed after registering the monitor data (word units) as in Example 2 of (2) (b) (Message wait time is 0 msec)


Check sum is calculated within this range.
Computer
ENQ
1 9 F F M Q 0 C 4
Check sum is calculated within this range.
ACK
1 9 F F
AJ71C24
STX
1 9 F F 1 2 3 4 0 0 5 0 0 0 6 4 0 7 6 4
ETX
2 3
Indicates that the data in D15 is 1234H (4660 in decimal).
Indicates that the data in W11E is 0050H (80 in decimal).
Indicates that the present value in T123 is 0064H (100 in decimal).
0 7 6 4
0 0 0 0 0 1 1 1 0 1 1 0 0 1 0 0
Y6F Y6E Y6D Y6C Y6B Y6A Y69 Y68 Y67 Y66 Y65 Y64 Y63 Y62 Y61 Y60

8.8 Extension File Register Read and Write

An extension file register refers to an empty area of the PC CPU user memory area used as a file register. The extension file register is used to store necessary data, results of the calculation for data processing executed using the SW0GHP-UTLPC-FN1 software package, and dedicated instructions for extension files used in the A2ACPU(S1) and A3ACPU.

8.8.1 ACPU common commands and addresses

(1) ACPU common commands used for read/write of extension file registers

Item	Command		Processing	Number of Points Processed per Communications	State of PC CPU		
	Symbol	ASCII Code			During STOP	During RUN	
						SW22 ON	SW22 OFF
Batch read	ER	45H, 52H	Reads from extension file registers (R) in units of 1 point.	64	o	o	o
Batch write	EW	45H, 57H	Writes to extension file registers (R) in units of 1 point.	64	o	o	x
Test (random write)	ET	45H, 54H	Specifies the extension file registers (R) in units of 1 point using block or device number and makes a random write.	10	o	o	x
Monitor data entry	EM	45H, 4DH	Sets the device numbers to be monitored in units of 1 point.	20	o	o	o
Monitor	ME	4DH, 45H	Monitors the extension file registers after monitor data entry.	—	o	o	o

Note : o Executable
x Not executable

(2) Extension file register addresses

(a) The extension file register comprises blocks number 0 to "n", with "n" varying according to the memory cassette. Block number "0" contains the number of points designated by the PC CPU parameters and each block with numbers "1" to "n" has 8192 points of registers.

Read/write is possible in the range of parameters designated in block number 0.

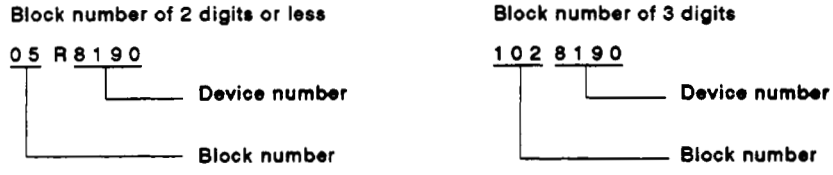
(b) The range of block numbers which can be designated varies according to the type of memory cassette and the PC CPU parameter setting.

The UTLP-FN1 Operating Manual or A2A(S1)/A3ACPU User's Manual give details.

(c) Each address is designated in 7 characters consisting of the block and device numbers.

- Block number of 2 digits or less:
  "Block number (2 digits)" + "R" + "Device number (4 digits)"
- Block number of 3 digits:
  "Block number (3 digits)" + "Device number (4 digits)

Example:



8.8.2 AnACPU dedicated commands and device numbers

(1) The AnACPU dedicated commands used for direct read and direct write of extension file registers are described below.

These dedicated commands are used to access the extension file register of block numbers 1 to 256 by directly designating the address, which begins with address 0 in block number 1, as the device number. The address numbers used to access the extension file register go from 0 to "the usable number of blocks x 8192 points".

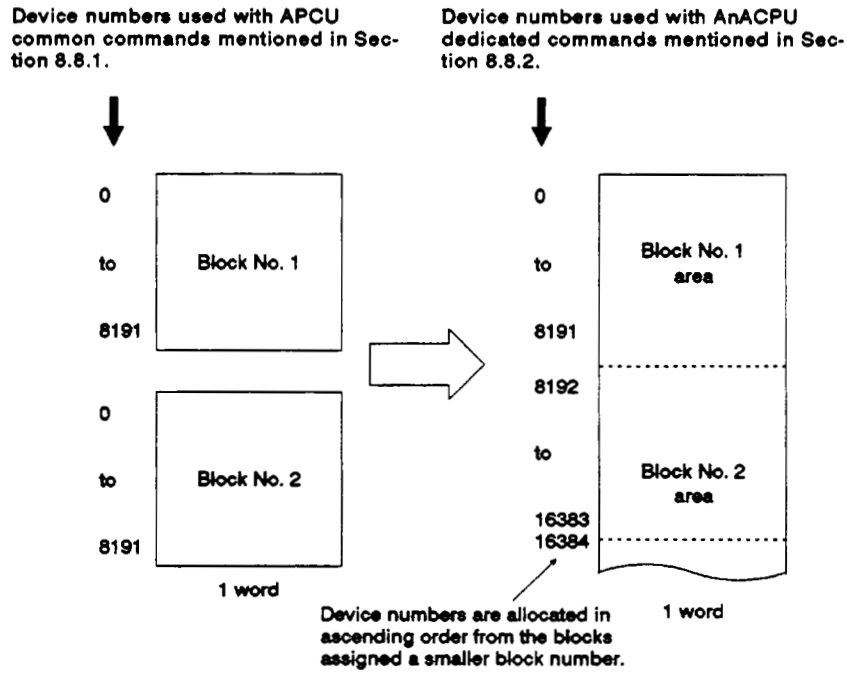
Item	Command		Processing	Number of Points Processed per Communications	State of PC CPU		
	Symbol	ASCII Code			During STOP	During RUN	
						SW22 ON	SW22 OFF
Direct read	NR	4EH, 52H	Reads in units of points (words) by designating the extension file register in successive numbers.	64 points	o	o	o
Direct write	NW	4EH, 57H	Writes data to the extension file register in units of points (words) by designating the extension file register in successive numbers.	64 points	o	o	x

Note : o Executable
x Not executable

(2) Device numbers of extension file registers

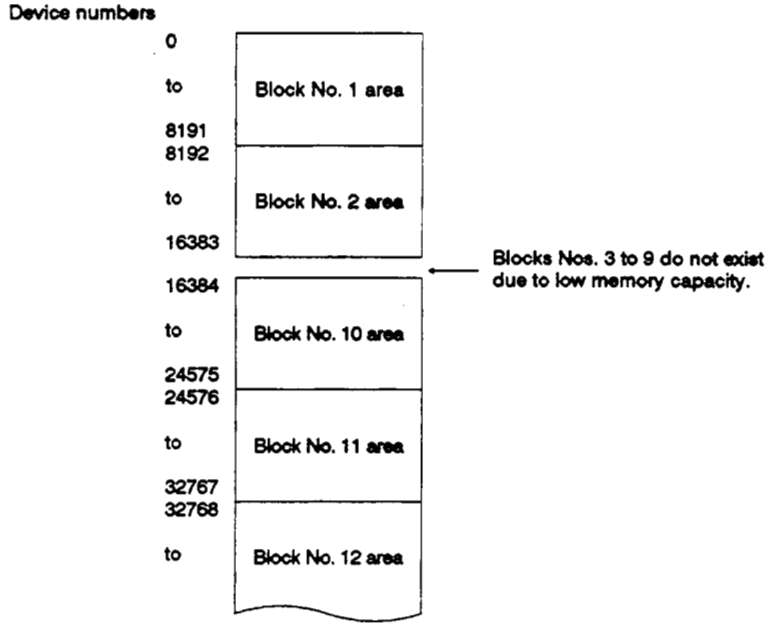
(a) Device number range

Range: 0 through [(the number of usable blocks x 8192) - 1]



The device numbers that can be designated vary according to the type of memory cassette and the PC CPU parameter setting. (The UTLP-FN1 Operating Manual or the A2A(S1)/A3A CPU User's Manual give details.)

For block numbers that do not exist in the memory cassette, device numbers are not allocated. In this case, the device numbers are allocated as indicated below, skipping non-existent block numbers.



(b) A device number is designated in 7 characters.

Designation example 1:
To designate R10 in block number 1:

0000010

A blank code (20H) can be used to express leading zeros (the underlined 0s in 0006200).

Designation example 2:
To designate R8 in block number 2:

0008200

POINTS

(1) The AnACPU dedicated commands NR and NW can only be used for read/write operations at the extension file registers of block numbers 1 to 256.

They can be used regardless of the parameter's file register setting.

(2) Use the commands described in Section 8.8.1 to access the parameter set file registers (R) or to access a file register by designating a block number.

(3) The following equation is used to calculate the head device number to be designated with the AnACPU dedicated commands NR and NW. (To designate device number "m" (0 to 8191) in the "n"th block ($n \geq 1$))

Head device number = $(n-1) \times 8192 + m$

REMARK

The range of device numbers (up to the 28th block) that can be designated with the NR or NW commands is shown below.

Device No.	Objective Block		Device No.	Objective Block	
0 to 8191	1st block	R0 to R8191	114688 to 122879	15th block	R0 to R8191
8192 to 16383	2nd block	R0 to R8191	122880 to 131071	16th block	R0 to R8191
16384 to 24575	3rd block	R0 to R8191	131072 to 139263	17th block	R0 to R8191
24576 to 32767	4th block	R0 to R8191	139264 to 147455	18th block	R0 to R8191
32768 to 40959	5th block	R0 to R8191	147456 to 155647	19th block	R0 to R8191
40960 to 49151	6th block	R0 to R8191	155648 to 163839	20th block	R0 to R8191
49152 to 57343	7th block	R0 to R8191	163840 to 172031	21st block	R0 to R8191
57344 to 65535	8th block	R0 to R8191	172032 to 180223	22nd block	R0 to R8191
65536 to 73727	9th block	R0 to R8191	180224 to 188415	23rd block	R0 to R8191
73728 to 81919	10th block	R0 to R8191	188416 to 196607	24th block	R0 to R8191
81920 to 90111	11th block	R0 to R8191	196608 to 204799	25th block	R0 to R8191
90112 to 98303	12th block	R0 to R8191	204800 to 212991	26th block	R0 to R8191
98304 to 106495	13th block	R0 to R8191	212992 to 221183	27th block	R0 to R8191
106496 to 114687	14th block	R0 to R8191	221184 to 229375	28th block	R0 to R8191

8.8.3 Precautions during extension file register read/write

(1) The extension file register is not used by A1 and A1NCPU.

This function is not available during communications between A1 or A1NCPU and the PC CPU.

(2) Some types of memory cassette loaded to the PC CPU are unable to detect an error (character area error 06H) if an attempt is made to read or write after specifying a block number which does not exist. In this case, data which is read may not be correct and writing such incorrect data may destroy the PC CPU user memory.

Always check the type of memory cassette and the parameter settings before using this function.

Type of Memory Cassette	Block Numbers Which do not Cause a Character Area Error (06H)		
	A0J2H, A2, A3CPU	A2NCPU, A3NCPU	A3H, A2A (S1) A3ACPU
A3NMCA-12	No. 10, No. 11		
A3NMCA-18	—	No. 10 to No. 28	
A3NMCA-24	—	No. 13 to No. 20	No. 13 to No. 28
A3NMCA-40	—		No. 21 to No. 28

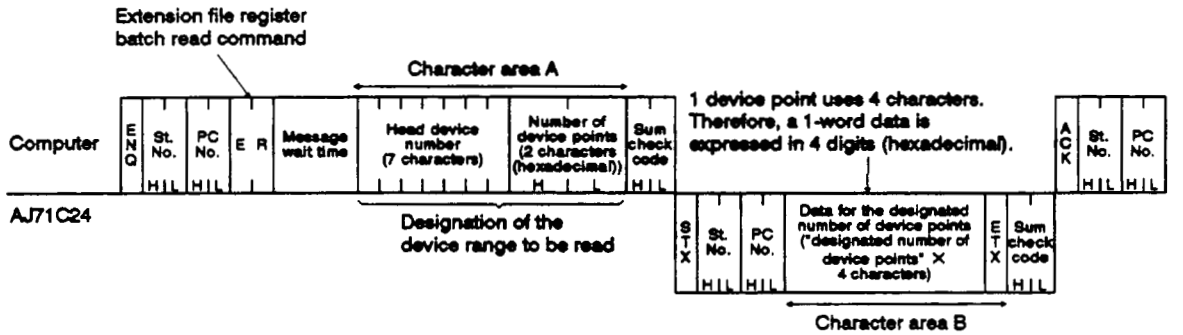
The UTLP-FN1 Operating Manual or the A2A(S1)/A3ACPU User's Manual give details.

8.8.4 Batch read of the extension file register (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



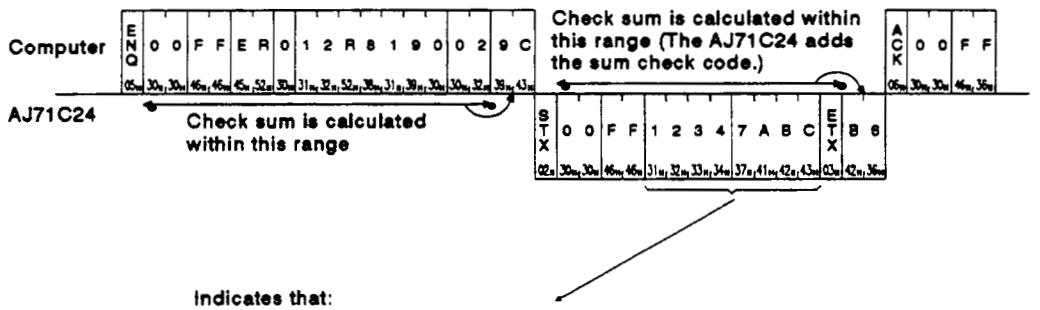
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤64
- (Head device number) + (number of device points) ≤ maximum device number

Designation Example

To read the data at 2 points of R8190 and R8191 of extension file register block number 12 in station number "0". (Message wait time is 0 msec)


Computer
ENQ 0 0 F F E R 0 1 2 R 8 1 9 0 0 2 9 C
Check sum is calculated within this range (The AJ71C24 adds the sum check code.)
ACK 0 0 F F
AJ71C24
Check sum is calculated within this range
STX 0 0 F F 1 2 3 4 7 A B C ETX B 6

Indicates that:

The content of R8190 of block Number 12 is 1234H (4660 in decimal)

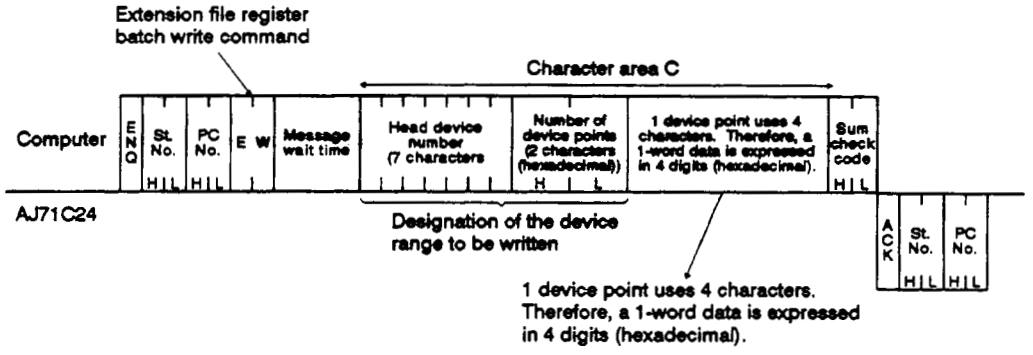
The content of R8191 of block Number 12 is 7ABCH (31420 in decimal)

8.8.5 Batch write of the extension file register (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.


Extension file register batch write command
Character area C
Computer
ENQ
St. No.
PC No.
E W
Message wait time
Head device number (7 characters
Number of device points (2 characters (hexadecimal))
1 device point uses 4 characters. Therefore, a 1-word data is expressed in 4 digits (hexadecimal).
Sum check code
H L
AJ71C24
Designation of the device range to be written
ACK
St. No.
PC No.
1 device point uses 4 characters.
Therefore, a 1-word data is expressed
in 4 digits (hexadecimal).

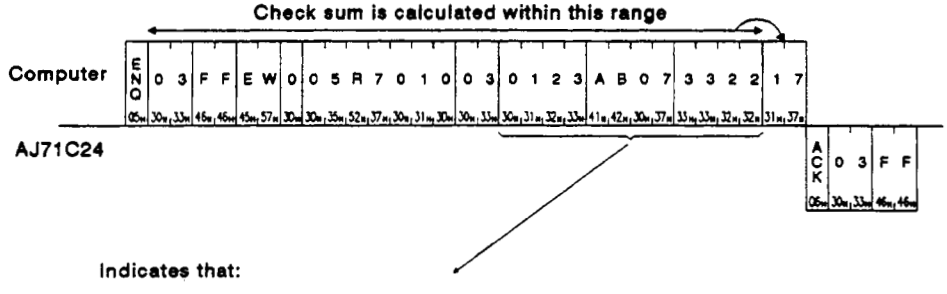
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 64
- (Head device number) + (number of device points) ≤ maximum device number

Designation Example

To write data to 3 points : R7010 to R7012 in the extension file register block number 05 in station number "3". (Message wait time is 0 msec)



Indicates that:

The content to be written to R7010 of block Number 05 is 0123H (291 in decimal)

The content to be written to R7011 of block Number 05 is AB07H (–21753 in decimal)

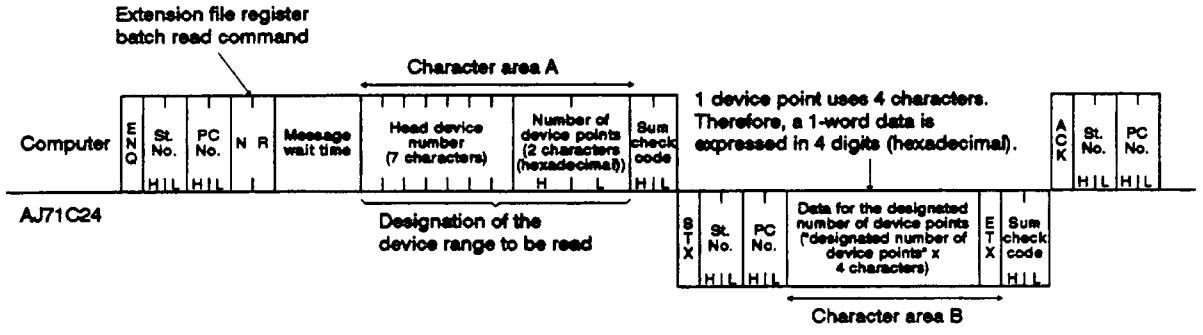
The content to be written to R7012 of block Number 05 is 3322H (13090 in decimal)

8.8.6 Direct read of the extension file register (AnACPU dedicated command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.


Extension file register batch read command
Character area A
Computer
ENQ
St. No.
PC No.
N R
Message wait time
Head device number (7 characters)
Number of device points (2 characters (hexadecimal))
Sum check code
H L
1 device point uses 4 characters. Therefore, a 1-word data is expressed in 4 digits (hexadecimal).
ACK
AJ71C24
Designation of the device range to be read
STX
Data for the designated number of device points ("designated number of device points" x 4 characters)
ETX
Character area B

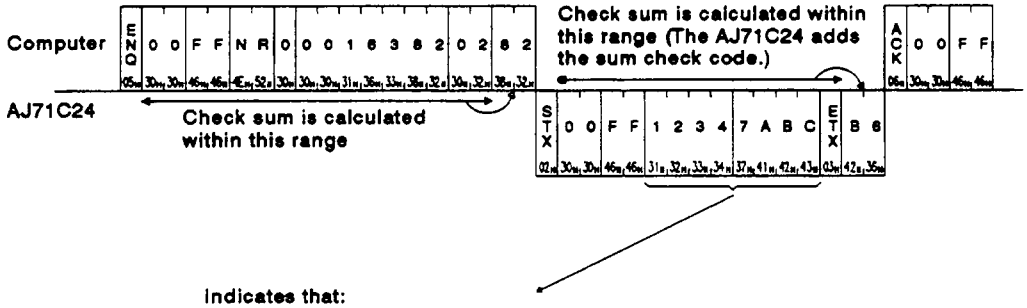
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 64
- (Head device number) + (number of device points) ≤ maximum device number

Designation Example

To read the data at points of R8190 and R8191 of extension file register block number 2 in station number "0". (Message wait time is 0 msec)


Computer
ENQ 0 0 F F N R 0 0 0 1 6 3 8 2 0 2 6 2
Check sum is calculated within this range (The AJ71C24 adds the sum check code.)
ACK 0 0 F F
AJ71C24
Check sum is calculated within this range
STX 0 0 F F 1 2 3 4 7 A B C ETX B 6

Indicates that:

The content of R8190 of block Number 2 is 1234H (4660 in decimal)

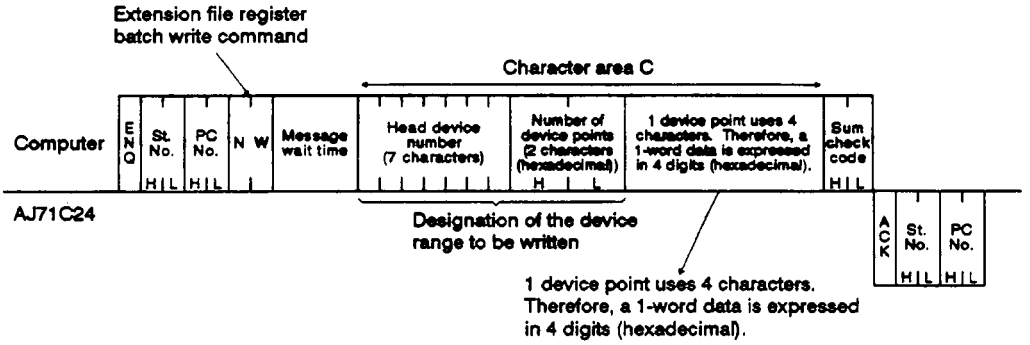
The content of R8191 of block Number 2 is 7ABCH (31420 in decimal)

8.8.7 Direct write to the extension file register (AnACPU dedicated command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.


Extension file register batch write command
Character area C
Computer
ENQ
St. No.
PC No.
N W
Message wait time
Head device number (7 characters)
Number of device points (2 characters (hexadecimal))
1 device point uses 4 characters. Therefore, a 1-word data is expressed in 4 digits (hexadecimal).
Sum check code
H L
AJ71C24
Designation of the device range to be written
ACK
St. No.
PC No.
1 device point uses 4 characters. Therefore, a 1-word data is expressed in 4 digits (hexadecimal).

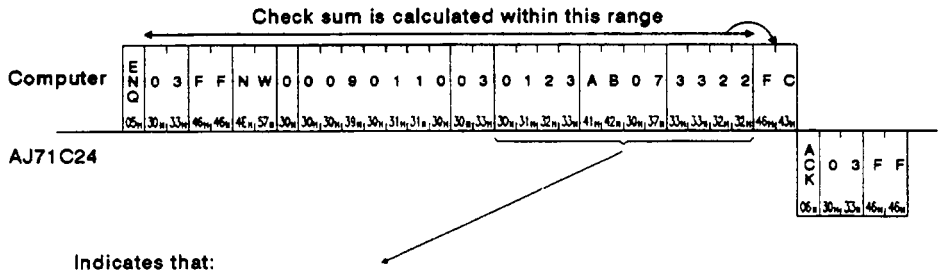
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 64
- (Head device number) + (number of device points) ≤ maximum device number

Designation Example

To write data to 3 points : R8190 and R8191 in extension file register block number 12 and R0 in block number 13, in station number "3". Assume that extension file register block number 9 does not exist. (Message wait time is 0 msec)



Indicates that:

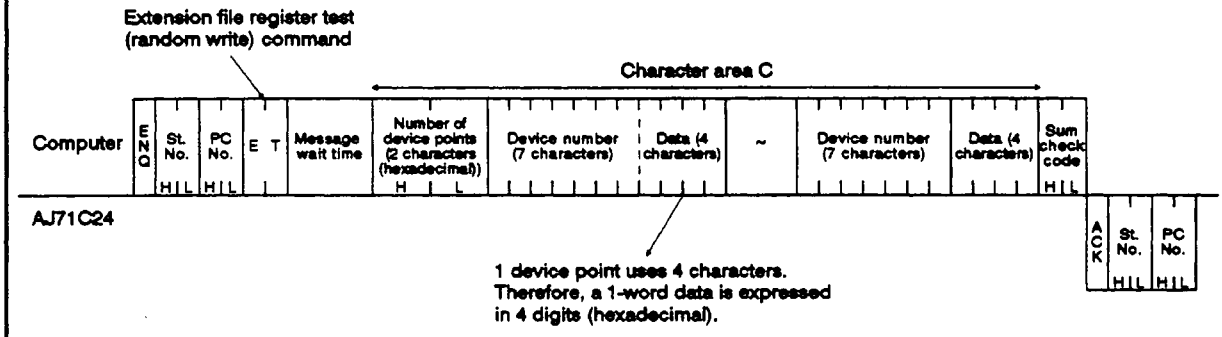
The content to be written to R8190 of block Number 12 is 0123H	(291 in decimal)
The content to be written to R8191 of block Number 12 is AB07H	(–21753 in decimal)
The content to be written to R0 of block Number 13 is 3322H	(13090 in decimal)

8.8.8 Testing (random write) the extension file register (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



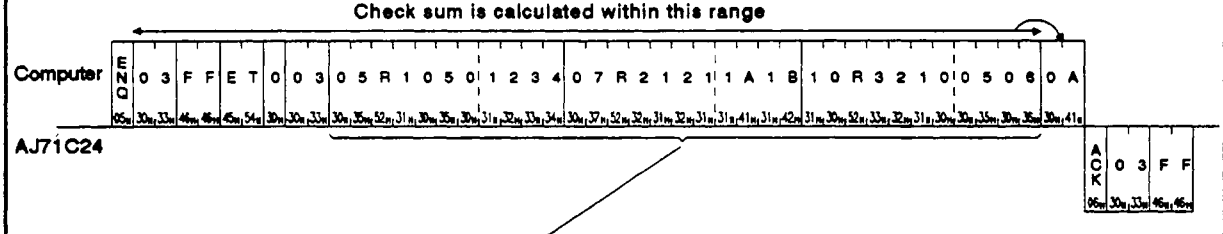
POINT

To designate the device range, the following condition must be met:

- 1 ≤ number of device points ≤ 10

Designation Example

To write data to 3 points : R1050 in extension file register block number 5, R2121 in block number 7, and R3210 in block number 10 in station number "3".
(Message wait time is 0 msec)


Check sum is calculated within this range
Computer
ENQ 0 3 F F E T 0 0 3 0 5 R 1 0 5 0 1 2 3 4 0 7 R 2 1 2 1 1 A 1 B 1 0 R 3 2 1 0 0 5 0 6 0 A
AJ71C24
ACK 0 3 F F

Indicates that:

The content to be written to R1050 of block number 05 is 1234H (4660 in decimal)

The content to be written to R2121 of block number 07 is 1A1BH (6683 in decimal)

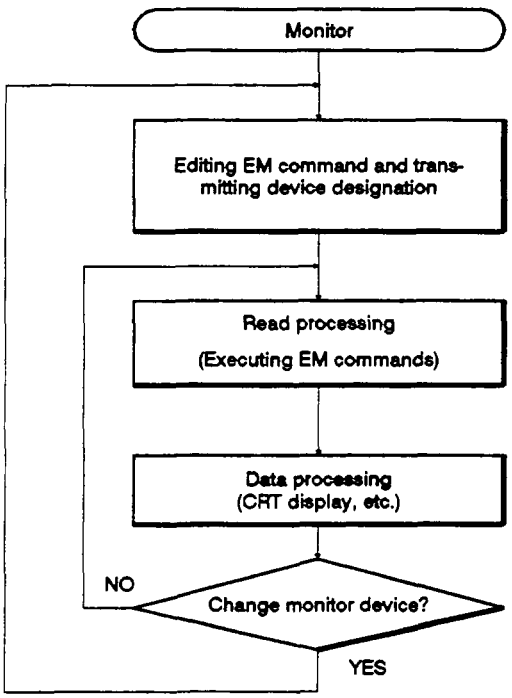
The content to be written to R3210 of block number 10 is 0506H (1286 in decimal)

8.8.9 Monitoring the extension file register

Monitor data registration is the function that registers the name and the number of the device to be monitored by the computer to the AJ71C24. The monitor is the function that (a) reads the data content of the device registered at the time the monitor read command is executed by the computer, and (b) executes the corresponding processing such as monitoring.

The device numbers must be consecutive when the device is read using the batch read (ER) or direct read (NR) command. However, when this function is used, it is possible to read and monitor the devices by designating the device numbers at random.

(1) Control procedure for monitoring



POINTS

(1) As the flowchart shows, monitor data registration must be executed before monitoring. Attempting to execute monitoring without registering the monitor data will cause a protocol error.

(2) The contents of the monitor data registration area are cleared when the power supply is turned OFF, the PC CPU is reset, or the mode is switched.

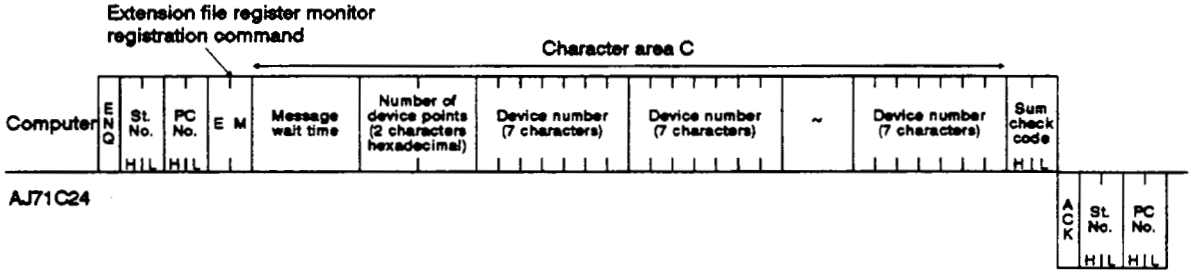
(3) For monitor registration, five types of registration are possible. They are device memory in bit units (BM or JM), device memory in word units (WM or QM) and the extension file register (EM).

(2) Registering Monitor data of the extension file register (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



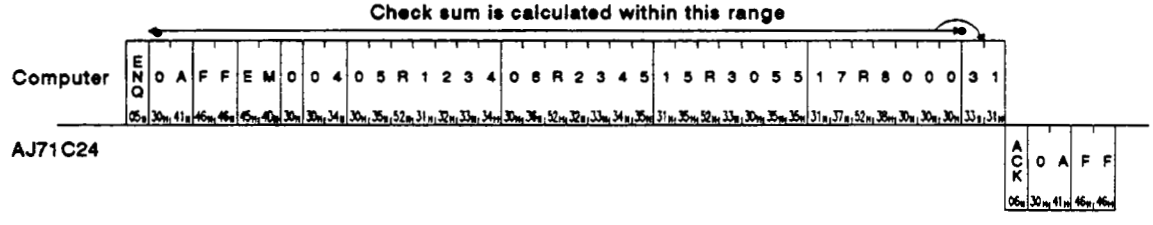
POINT

To designate the device range, the following condition must be met:

- 1 ≤ number of device points ≤ 20

Designation Example

To register monitor data for R1234 in extension file register block number 5, R2345 in block number 6, R3055 in block number 15, and R8000 in block number 17 in station number "10". (Message wait time is 0 msec)



POINT

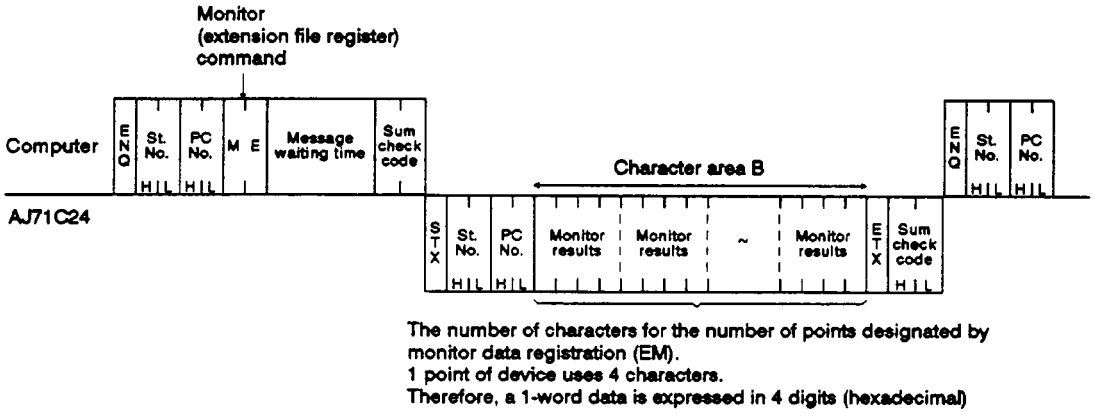
The station number is designated in hexadecimal. Therefore, the designation of station number 10 should be made in 0AH.

(3) Monitoring the extension file register (ACPU common command)

Designation Method

St. No. : Station number

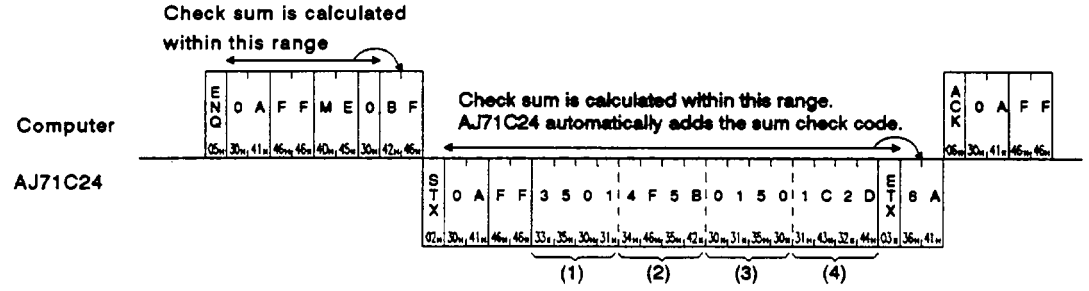
Designation in protocol 1 is shown below.



The number of characters for the number of points designated by monitor data registration (EM).
1 point of device uses 4 characters.
Therefore, a 1-word data is expressed in 4 digits (hexadecimal)

Designation Example

Monitoring after registering the monitor data (word units) as mentioned in item (2).
(Message wait time is 0 msec)



(1) the content of R1234 of extension file register block number 05 is 3501H (13569 in decimal),

(2) the content of R2345 of extension file register block number 06 is 4F5BH (20315 in decimal),

(3) the content of R3055 of extension file register block number 15 is 0150H (336 in decimal),

(4) the content of R8000 of extension file register block number 17 is 1C2DH (7213 in decimal),

8.9 Buffer Memory Read and Write

This function is used to read from and write to the AJ71C24 buffer memory. When this function is used, communications between the computer and AJ71C24 commences immediately when the computer sends a read or write request, without waiting for the PC CPU END processing. Therefore, the time T1, described in Section 8.5, is always equal to zero. The PC CPU carries out buffer memory read and write using TO and FROM instructions.

The method for specifying the control protocol, meanings, and examples for carrying out this function are shown below.

8.9.1 Commands and buffer memory

(1) ACPU common commands

Item	Command		Processing	Number of Points Processed per Communications	State of PC CPU		
	Symbol	ASCII Code			During STOP	During RUN	
						SW22 ON	SW22 OFF
Batch read	CR	43H, 52H	Reads from buffer memory.	64 words (128 bytes)	o	o	o
Batch write	CW	43H, 57H	Writes to buffer memory.				

Note : o .....Executable

(2) Buffer memory

Buffer memory addresses are 0H to 7FFH see (see Section 3.5).

One address consists of 1 word (16 bits).

Read and write are both executed in word units, regardless of the word/byte unit setting.

POINTS

(1) When accessing the user area in buffer memory simultaneously by using this function in the no-protocol mode (see Section 9) or the bidirectional mode (see Section 10), the buffer memory address in the following area should not be designated by the command described in item (1) in Section 8.9.1.

- No-protocol mode send area (or bidirectional mode send area)
- No-protocol mode receive area (or bidirectional mode receive area)
- On-demand area

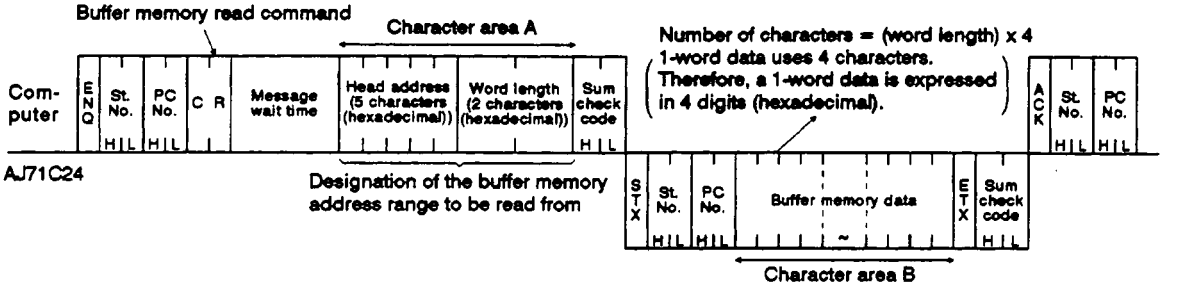
(2) Buffer addresses 100H to 11FH comprise the special applications area. The AJ71C24 will not operate correctly if any operations other than those described in the following sections are executed.

8.9.2 Reading data from buffer memory (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



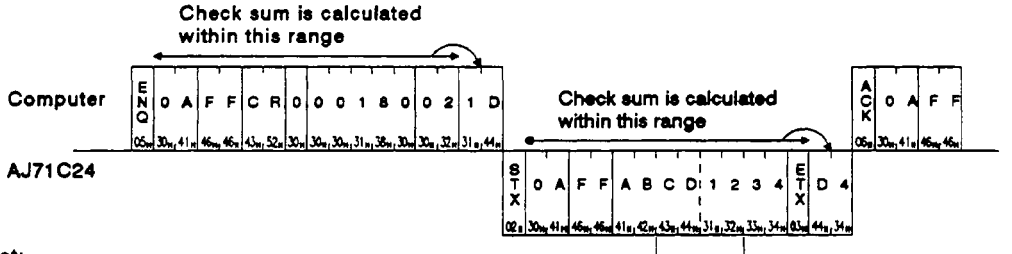
POINT

To designate the word length, the following conditions must be met:

- 1 ≤ word length ≤ 64
- (Head address) + (word length) – 1 ≤ maximum address number (7FFH)

Designation Example

To read 2-word data from buffer memory addresses 180H and 181H in the AJ71C24 of station number "10".
(Message wait time is 0 msec)


Check sum is calculated within this range
Computer
ENQ 0 A F F C R 0 0 0 1 8 0 0 2 1 D
Check sum is calculated within this range
ACK 0 A F F
AJ71C24
STX 0 A F F A B C D 1 2 3 4 ETX D 4

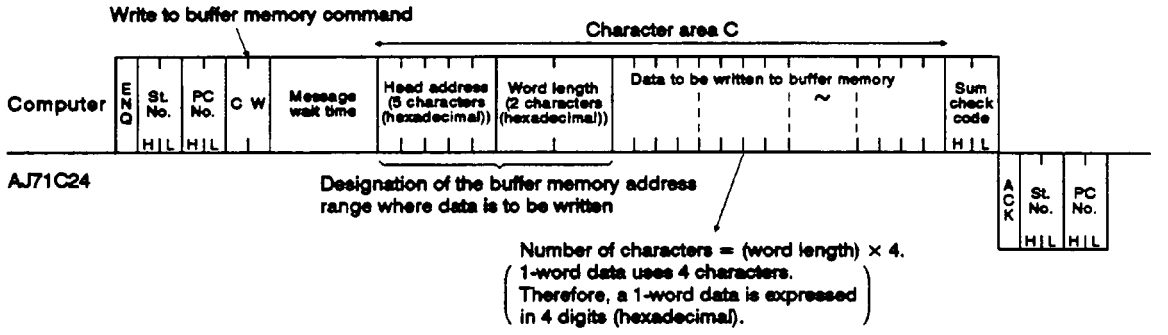
Indicates that:
The content of buffer memory address 180H is ABCDH (–21555 in decimal)
The content of buffer memory address 181H is 1234H (4660 in decimal)

8.9.3 Writing data to buffer memory (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.


Write to buffer memory command
Character area C
Computer
ENQ
St. No.
PC No.
C W
Message wait time
Head address (5 characters (hexadecimal))
Word length (2 characters (hexadecimal))
Data to be written to buffer memory
Sum check code
H L
AJ71C24
ACK
St. No.
PC No.
Designation of the buffer memory address range where data is to be written
Number of characters = (word length) × 4.
(1-word data uses 4 characters. Therefore, a 1-word data is expressed in 4 digits (hexadecimal).)

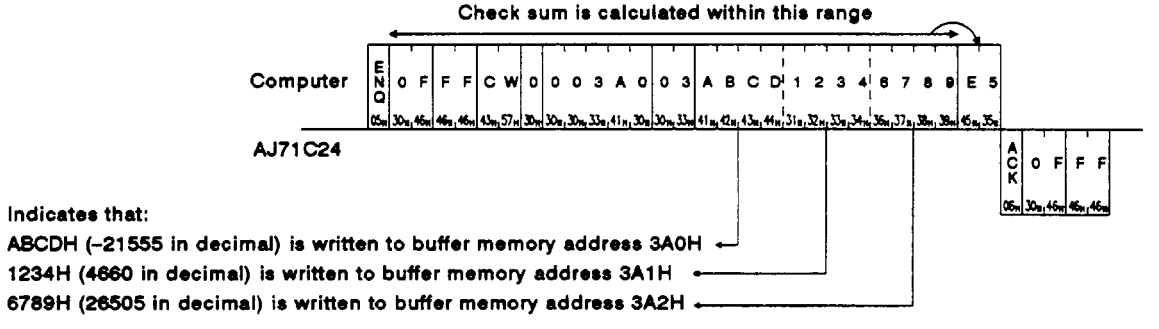
POINT

To designate the word length, the following conditions must be met:

- 1 ≤ word length ≤ 64
- (Head address) + (word length) − 1 ≤ maximum address number (7FFH)

Designation Example

To write 3-word data to buffer memory address 3A0H to 3A2H in the AJ71C24 of station number "15".
(Message wait time is 0 msec)


Check sum is calculated within this range
Computer
ENQ 0 F F F C W 0 0 0 3 A 0 0 3 A B C D 1 2 3 4 6 7 8 9 E 5
AJ71C24
ACK 0 F F F
Indicates that:
ABCDH (–21555 in decimal) is written to buffer memory address 3A0H
1234H (4660 in decimal) is written to buffer memory address 3A1H
6789H (26505 in decimal) is written to buffer memory address 3A2H

8.10 Special Function Module Buffer Memory Read and Write

8.10.1 Commands and designation

(1) ACPU common commands

Item	Command		Processing	Number of Points Processed per Communications	State of PC CPU		
	Sym-bol	ASCII Code			During STOP	During RUN	
						SW22 ON	SW22 OFF
Batch read	TR	54H, 52H	Reads from special function module buffer memory.	64 words (128 bytes)	o	o	o
Batch write	TW	54H, 57H	Writes to special function module buffer memory.		o	o	x

Note : o .....Executable
x .....Not executable

(2) Linkable special function modules, buffer memory head address, and module numbers

See the list shown in Appendix 7.

(3) Special-function module buffer memory

The special-function module buffer memory is comprised of 16-bit (one word) addresses. Read and write of the special-function module buffer memory is executed by TO and FROM instructions transmitted between the PC CPU and special-function module.

When the computer reads from and writes to the special-function module buffer memory via the AJ71C24, it is done in byte units (1 address = 8 bits).

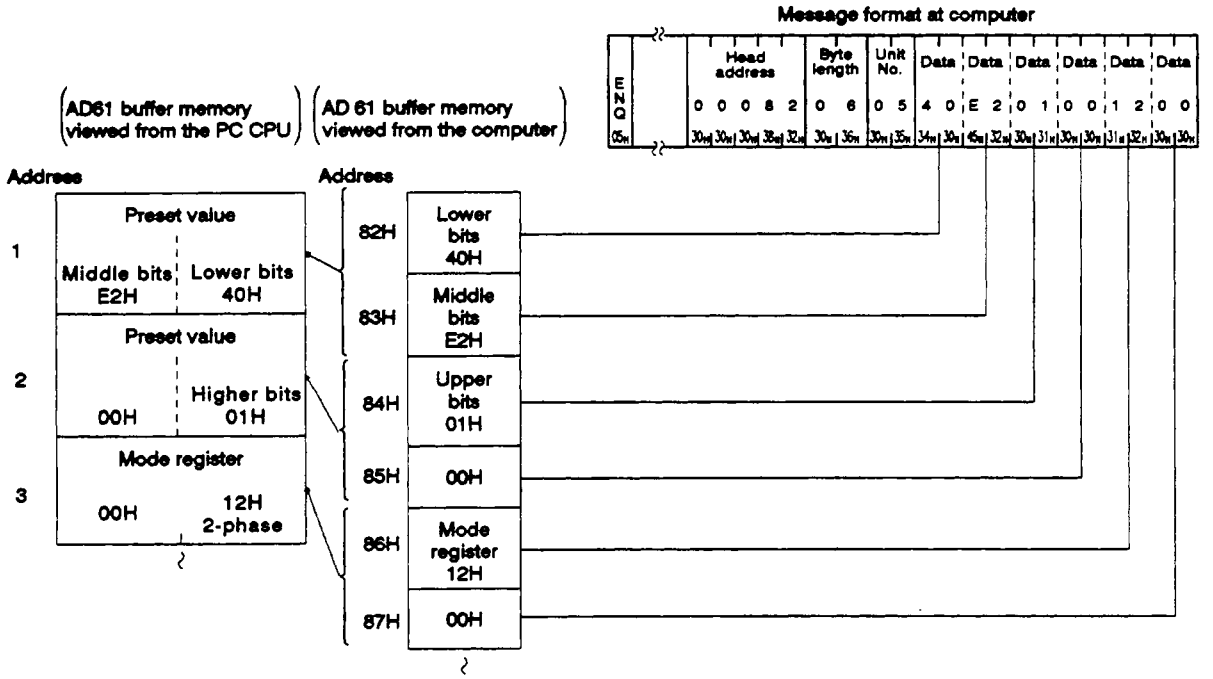
The addresses specified in the computer (hexadecimal) are converted from FROM/TO instruction addresses as shown below:

Designated address (hexadecimal) = Module head address + [(FROM/TO instruction address × 2) converted into hexadecimal]

Example: To designate AD61 high-speed counter module FROM/TO instruction address 1 (CH.1 preset value).

Specified address 82H = FROM/TO instruction address 1 × 2 (2H) + Head address (80H)

The data format when the computer makes a read or write to or from the special-function module buffer memory via the AJ71C24, is explained below using the AD61 module as an example.



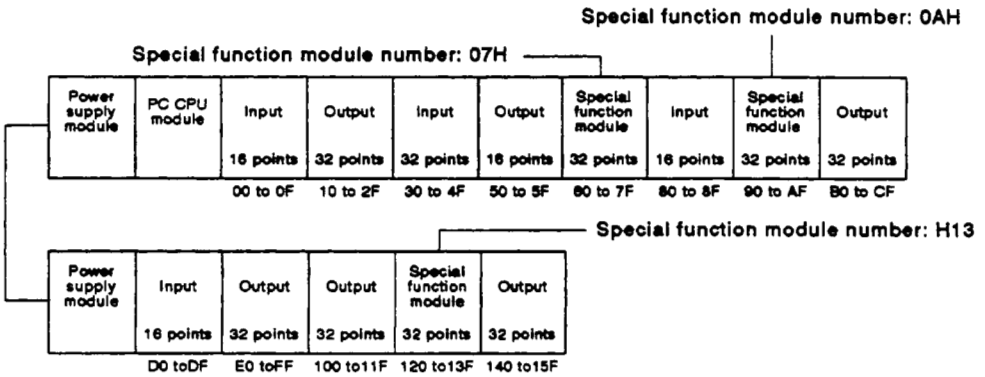
POINT

The buffer memory of each special-function module has its read and write area, read-only and write-only areas, and areas reserved for OS use, which are not available to the use. See the manual for each module before using the buffer memory.

PC CPU or special-function module errors may occur if reading or writing is not done correctly.

8.10.2 Special function module numbers using control protocols

(1) The special function module numbers designated by using control protocols are the upper 2 digits of the last special function module I/O address expressed in 3 digits.

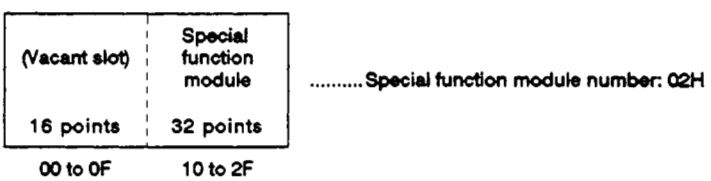


(2) Precautions with special function modules occupying two slots

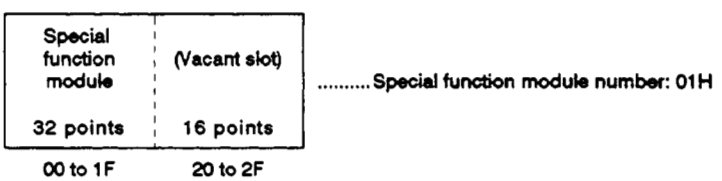
For special function modules occupying two slots, the number of points occupied by each slot is fixed for each module. The special function module number is the upper 2 digits of the last address of the slot allocated to the special function module.

The User's Manual for each special function module gives details about the allocation of slots to each module.

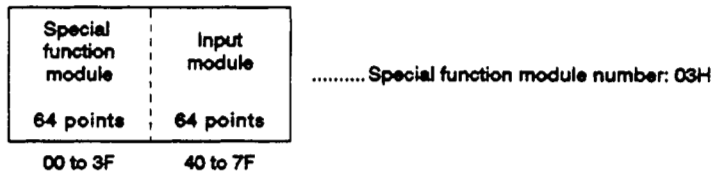
(a) Modules with the front slot allocated as the vacant slot (AD72, A84AD, etc.)



(b) Modules with the rear slot allocated as the empty slot (A61LS, etc.)



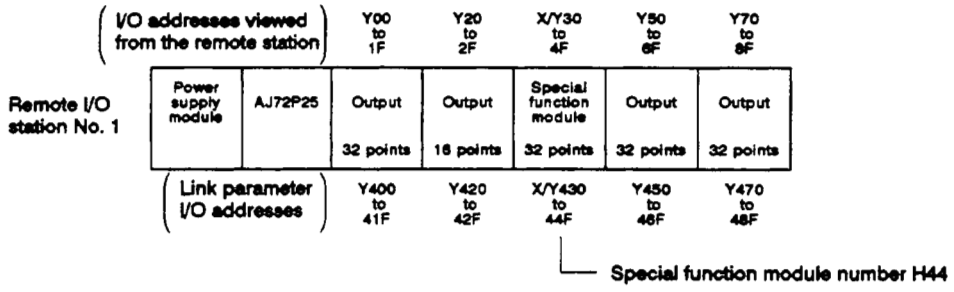
(c) Modules with the special function module allocation and I/O allocation mixed (A81CPU, etc.)



(3) Module numbers of special-function modules at MELSECNET (II) remote I/O stations

The module numbers of special function modules at MELSECNET (II) remote stations are determined by link parameters setting at the MELSENET (II) master station.

L/R	M ← L		M → R	M ← R	M → L/R		M ← L/R	
NO.	B	W	W	W	Y	X/Y	X	Y/X
R1	----	----	29C–309	0F9–15E	400–48F	000–08F	430–44F	030–04F
R2	----	----	215–24F	080–0A3	510–67F	010–17F	500–65F	000–15F
R3	----	----	1B6–214	15F–1B5	270–32F	050–10F	220–28F	000–06F
	–	–	–	–	–	–	–	–
	–	–	–	–	–	–	–	–
	–	–	–	–	–	–	–	–
	–	–	–	–	–	–	–	–
	–	–	–	–	–	–	–	–

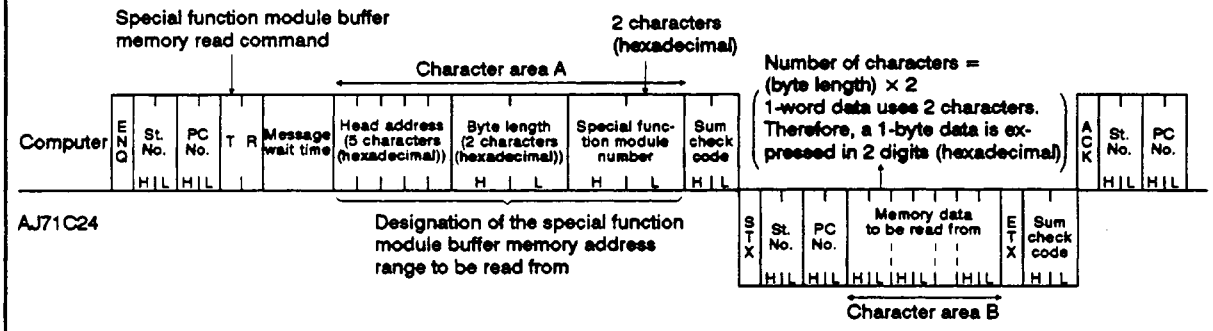


8.10.3 Reading data from the special-function module buffer memory (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.


Special function module buffer memory read command
2 characters (hexadecimal)
Character area A
Number of characters = (byte length) × 2
1-word data uses 2 characters. Therefore, a 1-byte data is expressed in 2 digits (hexadecimal)
Computer
ENQ
St. No.
PC No.
T R
Message wait time
Head address (5 characters (hexadecimal))
Byte length (2 characters (hexadecimal))
Special function module number
Sum check code
ACK
AJ71C24
Designation of the special function module buffer memory address range to be read from
STX
Memory data to be read from
ETX
Character area B

POINTS

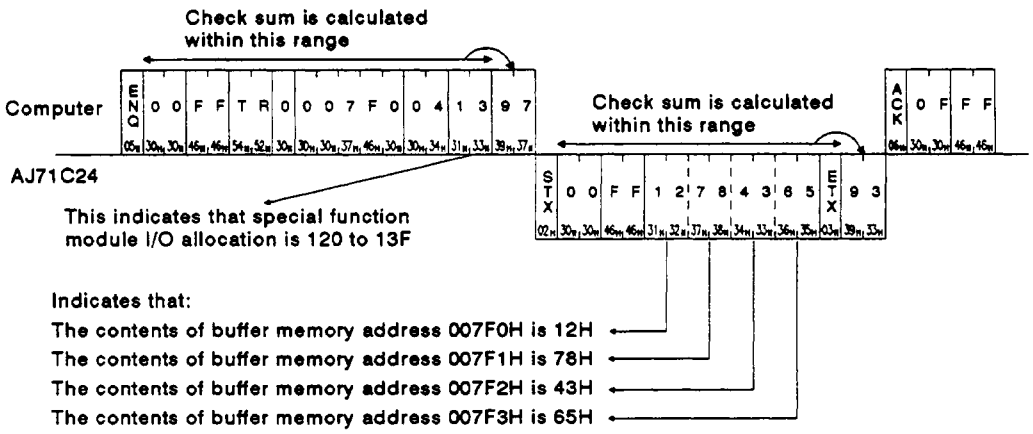
(1) To designate the byte length, the following condition must be met:

- 1 ≤ byte length ≤ 128

(2) With some special function modules, 2 or 3 bytes are used to express the data. Therefore, designate the byte length by referring to the manuals for each individual module.

Designation Example

To read the data from buffer memory address 07F0H to 07F3H (4 bytes) of the special-function module (module number 13H) loaded at I/O numbers 120 to 13F in station number "0". (Message wait time is 0 msec)

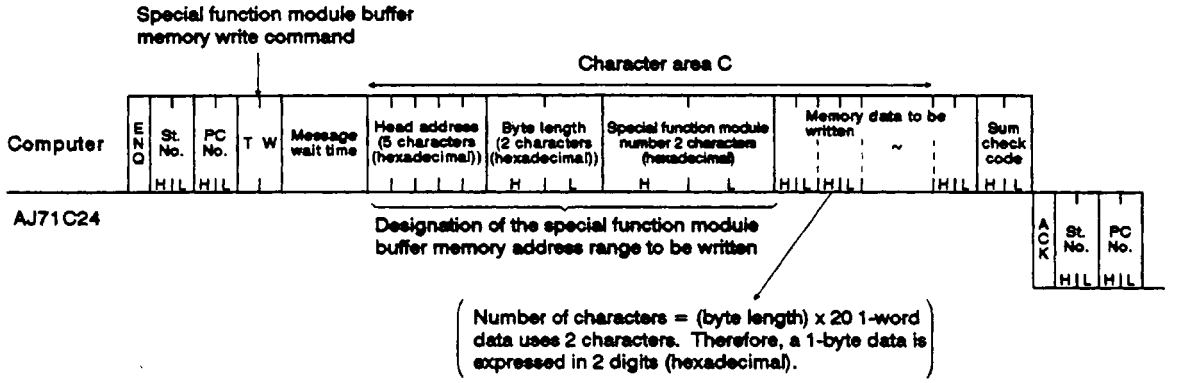

Check sum is calculated within this range
Computer
ENQ 0 0 F F T R 0 0 0 7 F 0 0 4 1 3 9 7
Check sum is calculated within this range
ACK 0 F F F
AJ71C24
STX 0 0 F F 1 2 7 8 4 3 6 5 ETX 9 3
This indicates that special function module I/O allocation is 120 to 13F
Indicates that:
The contents of buffer memory address 007F0H is 12H
The contents of buffer memory address 007F1H is 78H
The contents of buffer memory address 007F2H is 43H
The contents of buffer memory address 007F3H is 65H

8.10.4 Writing data to the special function module buffer memory (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.


Special function module buffer memory write command
Character area C
Computer
ENQ
St. No.
PC No.
T W
Message wait time
Head address (5 characters (hexadecimal))
Byte length (2 characters (hexadecimal))
Special function module number 2 characters (hexadecimal)
Memory data to be written
Sum check code
AJ71C24
ACK
St. No.
PC No.
Designation of the special function module buffer memory address range to be written
Number of characters = (byte length) x 20 1-word data uses 2 characters. Therefore, a 1-byte data is expressed in 2 digits (hexadecimal).

POINTS

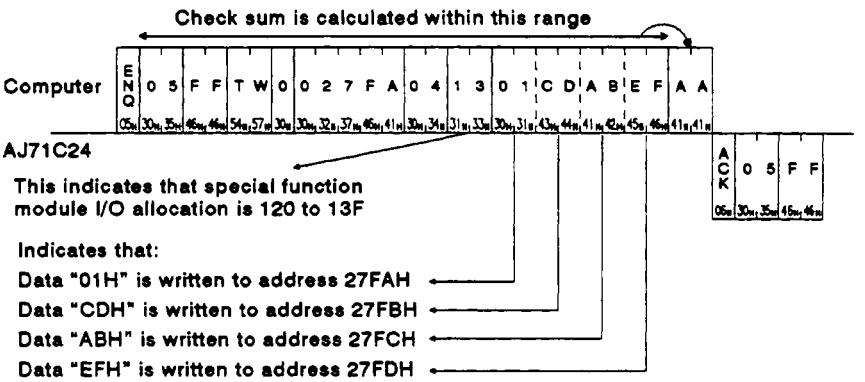
(1) To designate the byte length, the following condition must be met:

- 1 ≤ byte length ≤ 128

(2) With some special function modules, 2 or 3 bytes are used to express the data. Therefore, designate the byte length by referring to the manuals for each individual module.

Designation Example

To write the data to buffer memory address 27FAH to 27FDH (4 bytes) of the special-function module (module number 13H) loaded at I/O numbers 120 to 13F in station number "5". (Message wait time is 0 msec)


Check sum is calculated within this range
Computer
ENQ 0 5 F F T W 0 0 2 7 F A 0 4 1 3 0 1 C D A B E F A A
AJ71C24
ACK 0 5 F F
This indicates that special function module I/O allocation is 120 to 13F
Indicates that:
Data "01H" is written to address 27FAH
Data "CDH" is written to address 27FBH
Data "ABH" is written to address 27FCH
Data "EFH" is written to address 27FDH

8.11 Remote Run/Stop of PC CPU and Reading PC CPU Model Name

8.11.1 Commands

(1) ACPU common commands

Item	Command		Processing	State of PC CPU		
	Symbol	ASCII Code		During STOP	During RUN	
					SW22 ON	SW22 OFF
Remote RUN	RR	52H, 52H	Requests remote RUN of PC CPU.	o	o	o
Remote STOP	RS	52H, 53H	Requests remote STOP of PC CPU.	o	o	o
PC CPU modle mode	PC	50H, 43H	Reads if the PC CPU is model A1N, A2N, A3N, A3H or AJ72P25/R25.	o	o	o

Note : o.....Executable

8.11.2 Remote RUN/STOP

(1) Remote RUN/STOP control

(a) RUN, STOP, PAUSE and STEP-RUN states are produced by the following combinations of PC CPU key switch positions and computer commands.

		PC CPU Key Switch Position			
		RUN	STOP	PAUSE	STEP-RUN
Command from computer	Remote RUN	RUN	STOP	PAUSE	STEP-RUN
	Remote STOP	STOP	STOP	STOP	STOP

REMARK

(a) When a PC CPU is stopped by the remote STOP command given by an external computer, that PC CPU cannot be put into the RUN state by the computer connected to the PC CPU.

(b) The clearing of data memories on receiving a remote RUN instruction depends on the states of special relays M9016 and M9017 as shown below.

Special Relay		Data Memory State
M9016	M9017	
OFF	OFF	PC CPU enters the RUN state without clearing remote STOP data.
OFF	ON	Remote STOP data is cleared outside the latch range set in parameters. (In this case, Link X image is not cleared.)
ON	ON/OFF	PC CPU enters the RUN state after data memory is cleared.

REMARK

Always reset special relays M9016 and M9017 when data memory clearing is not required.

POINT

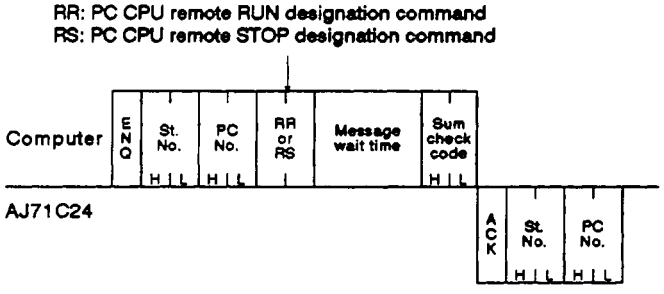
After operations remote RUN/STOP control from the computer are completed, the remote data will be lost if the power supply is turned OFF or the PC CPU is reset.

(2) Remote RUN/STOP designations and designation examples (ACPU common command)

Designation Method

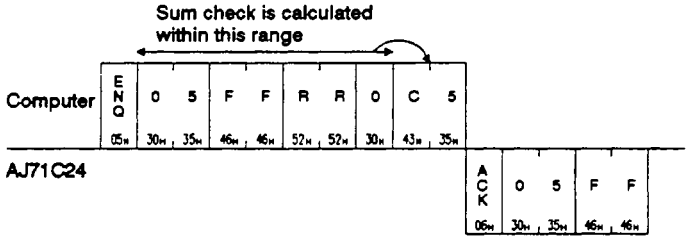
St. No. : Station number

Designation in protocol 1 is shown below.

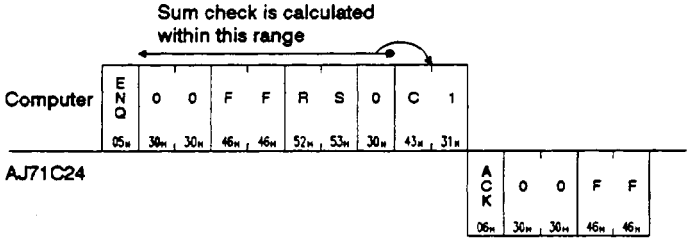


Designation Examples

Example 1: Remote RUN control of PC CPU in station number "5" (Message wait time is 0 msec)


Sum check is calculated within this range
Computer
ENQ 0 5 F F R R 0 C 5
05H 30H, 35H 46H, 46H 52H, 52H 30H 43H, 35H
AJ71C24
ACK 0 5 F F
06H 30H, 35H 46H, 46H

Example 2: Remote STOP control of PC CPU in station number "0" (Message wait time is 0 msec)


Sum check is calculated within this range
Computer
ENQ 0 0 F F R S 0 C 1
05H 30H, 30H 46H, 46H 52H, 53H 30H 43H, 31H
AJ71C24
ACK 0 0 F F
06H 30H, 30H 46H, 46H

8.11.3 Reading PC CPU model name

(1) PC CPU model name and corresponding codes

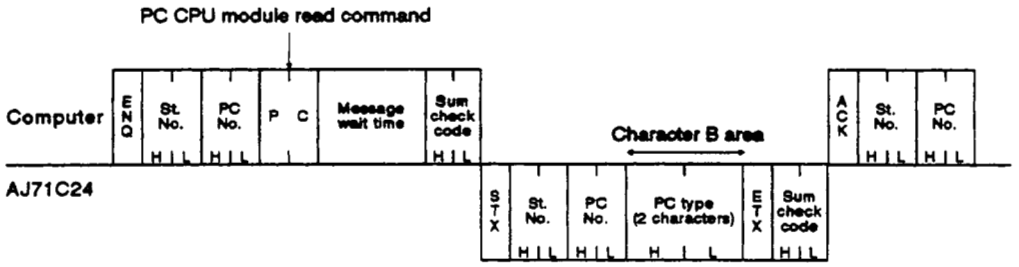
PC CPU Model Name	Code To Be Read (Hexadecimal)	PC CPU Model Name	Code To Be Read (Hexadecimal)
A0J2HCPU	98H	A2CCPU	9AH
A1CPU, A1NCPU	A1H	A3CPU, A3NCPU	A3H
A1SCPU	98H	A3ACPU	94H
A2CPU(-S1), A2NCPU(-S1)	A2H	A3HCPU, A3MCPU	A4H
A2ACPU	92H	A73CPU	A3H
A2ACPU-S1	93H	AJ72P25/R25	ABH

(2) Reading PC CPU model name (ACPU common commands)

Designation Method

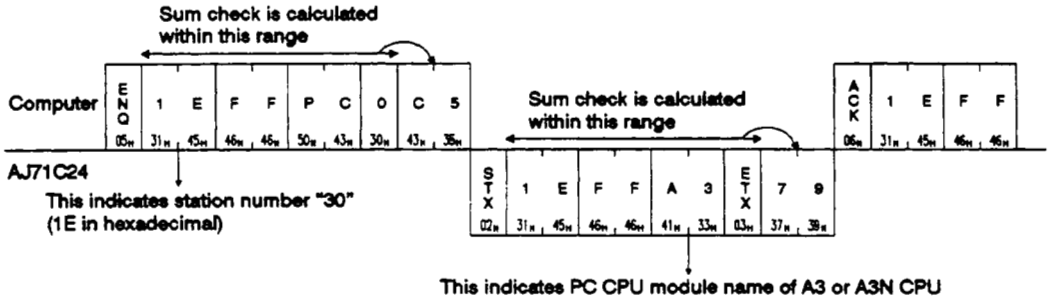
St. No. : Station number

Designation in protocol 1 is shown below.



Designation Example

To read PC CPU model name at station number "30" (Message wait time is 0 msec)



8.12 Program Read/Write

This function is used to transfer all types of programs (main and sub-sequence programs, microcomputer main and sub programs), parameters and comment data from the PC CPU and store them in the computer. The computer then carries out the appropriate controls by writing programs, parameters, and comment data to the PC CPU.

8.12.1 Precautions during program read/write

(1) When reading programs that have been written to the PC CPU, read all sequence programs, microcomputer programs, parameter data, and comment data from all areas.

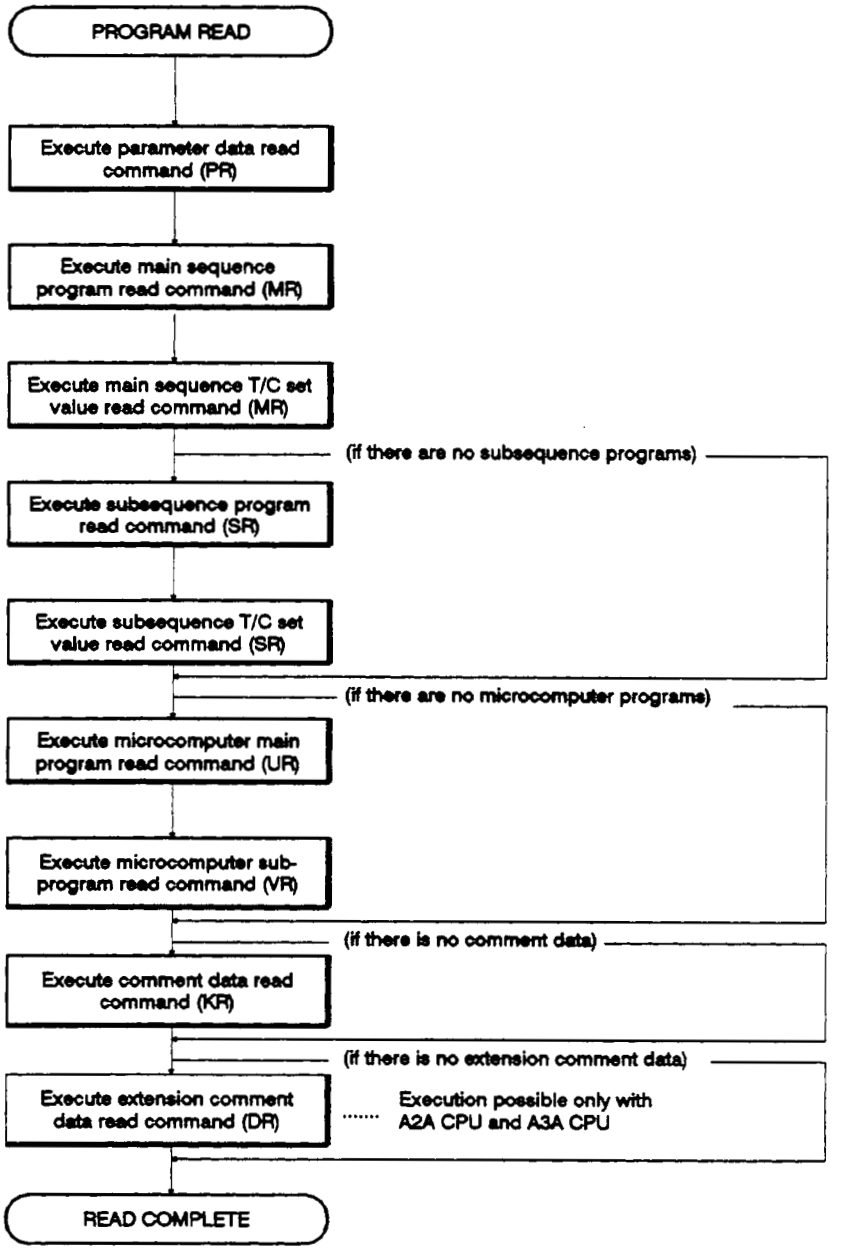
When writing programs, write all stored data to the PC CPU. If all areas have not been written to, the PC CPU will not work correctly.

(2) Before writing programs, write parameter data and execute a parameter analysis request. Otherwise, the parameters in the PC CPU user memory will be changed but the parameters stored in the work area by the ACPU for operation will remain unchanged. Therefore, if a peripheral device is loaded and operated after the parameters are changed, processing will be carried out with the previous parameters, which are still stored in the work area.

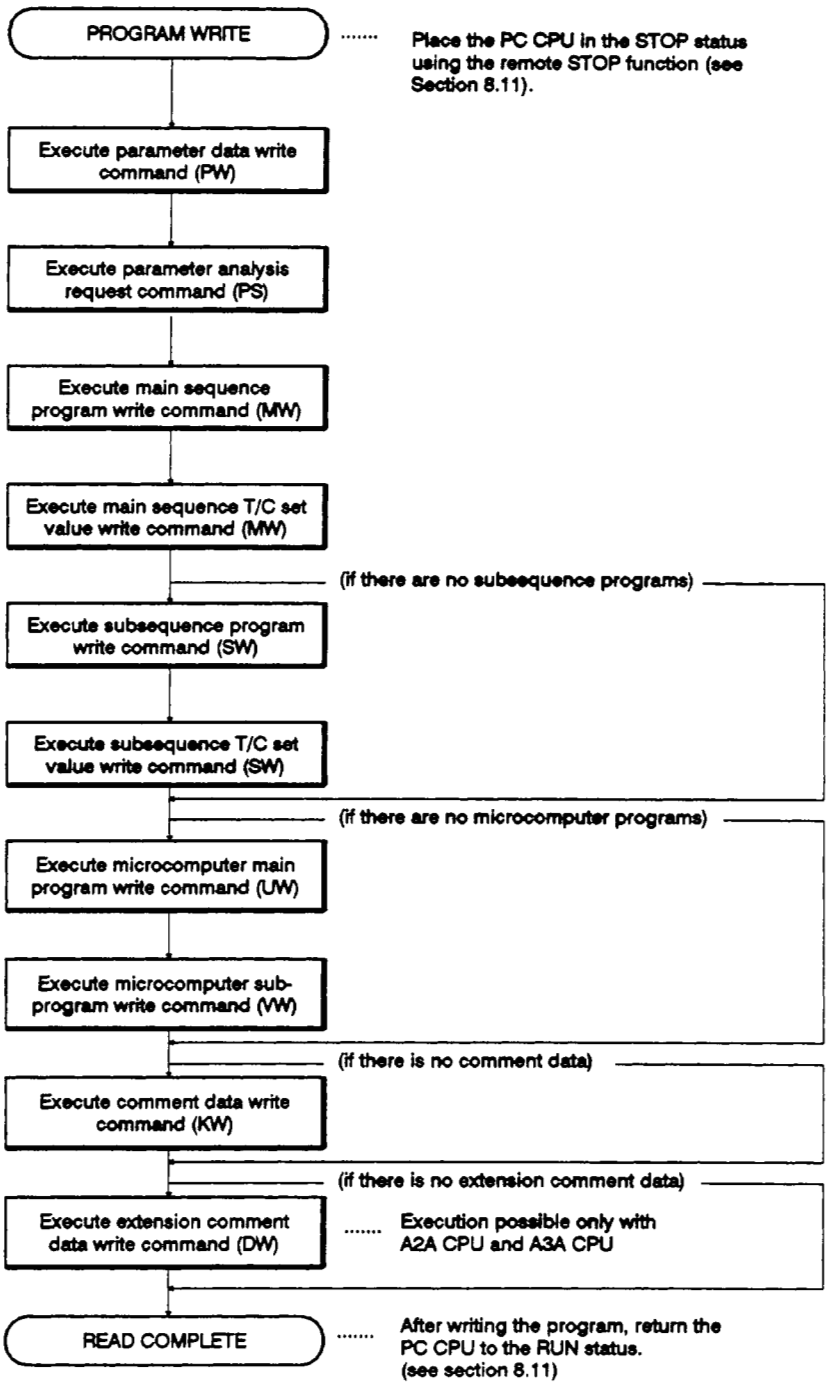
(3) The number of points which can be processed per communications is fixed. When reading or writing data, divide the data into several groups to read or write the entire area. Parameter data should be divided into 3K bytes. Other data shoule be divided into units of data determined by parameter setting.

8.12.2 Program read/write control procedures

(1) Reading


PROGRAM READ
Execute parameter data read command (PR)
Execute main sequence program read command (MR)
Execute main sequence T/C set value read command (MR)
(if there are no subsequence programs)
Execute subsequence program read command (SR)
Execute subsequence T/C set value read command (SR)
(if there are no microcomputer programs)
Execute microcomputer main program read command (UR)
Execute microcomputer sub-program read command (VR)
(if there is no comment data)
Execute comment data read command (KR)
(if there is no extension comment data)
Execute extension comment data read command (DR)
Execution possible only with A2A CPU and A3A CPU
READ COMPLETE

(2) Writing


PROGRAM WRITE
Place the PC CPU in the STOP status using the remote STOP function (see Section 8.11).
Execute parameter data write command (PW)
Execute parameter analysis request command (PS)
Execute main sequence program write command (MW)
Execute main sequence T/C set value write command (MW)
(if there are no subsequence programs)
Execute subsequence program write command (SW)
Execute subsequence T/C set value write command (SW)
(if there are no microcomputer programs)
Execute microcomputer main program write command (UW)
Execute microcomputer sub-program write command (VW)
(if there is no comment data)
Execute comment data write command (KW)
(if there is no extension comment data)
Execute extension comment data write command (DW)
Execution possible only with A2A CPU and A3A CPU
READ COMPLETE
After writing the program, return the PC CPU to the RUN status. (see section 8.11)

8.12.3 Parameter memory read/write

(1) Commands and addresses

(a) ACPU common commands

Item	Command		Processing	Number of Points Processed per Communication	PC CPU State		
	Symbol	ASCII code			During STOP	During RUN	
						SW22 ON	SW22 OFF
Batch read	PR	50H, 52H	Reads parameters.	128 bytes	o	o	o
Batch write	PW	50H, 57H	Writes parameters.		o	x	x
Analysis request	PS	50H, 53H	Causes the PC CPU to acknowledge and check rewritten parameters.		o	x	x

Note : o.....Executable
x.....Unavailable

(b) Parameter addresses

There are 3K bytes of parameter memory, addresses 00000H to 00BFFH. For addresses, use 5-digit ASCII (hexadecimal).

POINT

After changing parameters, always call the parameter analysis request command (PS).

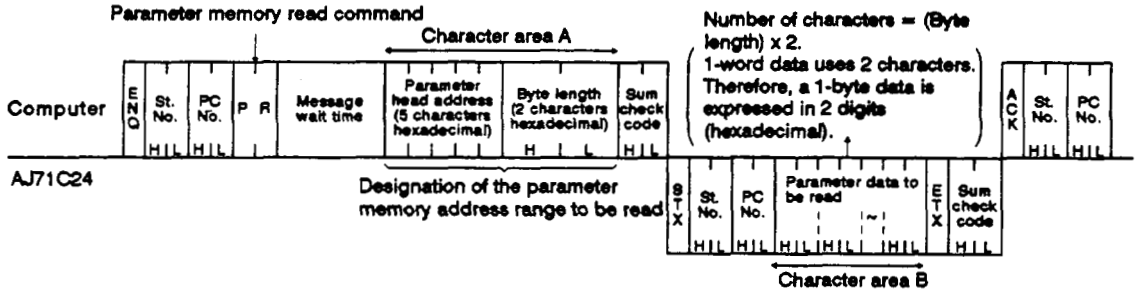
If this is not done, the parameters in PC CPU user memory will be changed but the parameters stored in the work area by the ACPU for operation will remain unchanged. Therefore, if a peripheral device is loaded and operated after the parameters are changed, processing will be executed with the previous parameters, which are still stored in the work area.

(2) Parameter memory batch read (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



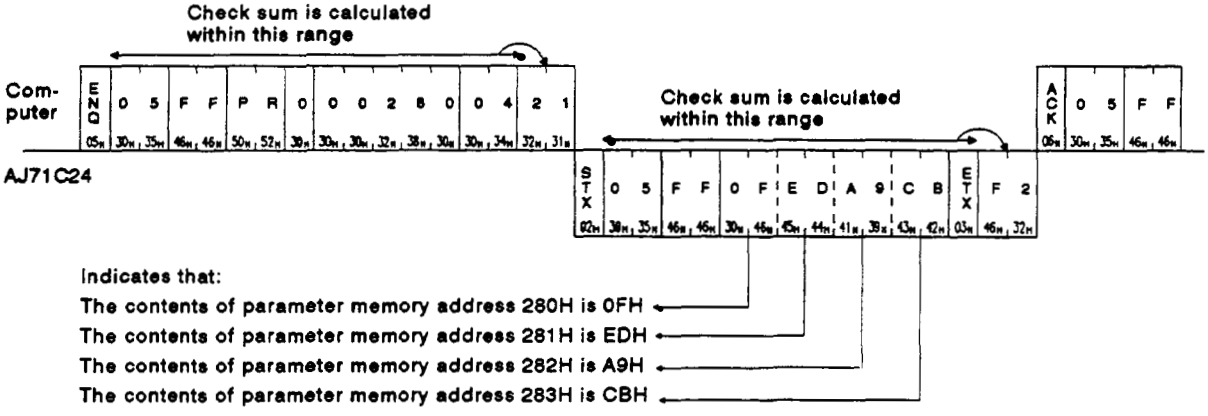
POINT

To designate the byte length, the following condition must be met:

- 1 ≤ byte length ≤ 128

Designation Example

To read 4-byte parameter data in parameter memory addresses 280H to 283H of the PC CPU in station number "5". (Message wait time is 0 msec)

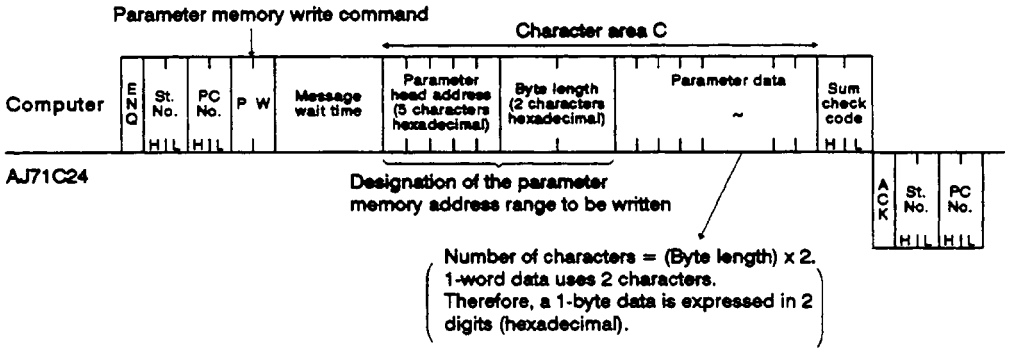

Check sum is calculated within this range
Com-puter
ENQ 0 5 F F P R 0 0 0 2 8 0 0 4 2 1
Check sum is calculated within this range
ACK 0 5 F F
AJ71C24
STX 0 5 F F 0 F E D A 9 C B ETX F 2
Indicates that:
The contents of parameter memory address 280H is 0FH
The contents of parameter memory address 281H is EDH
The contents of parameter memory address 282H is A9H
The contents of parameter memory address 283H is CBH

(3) Parameter memory batch write (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



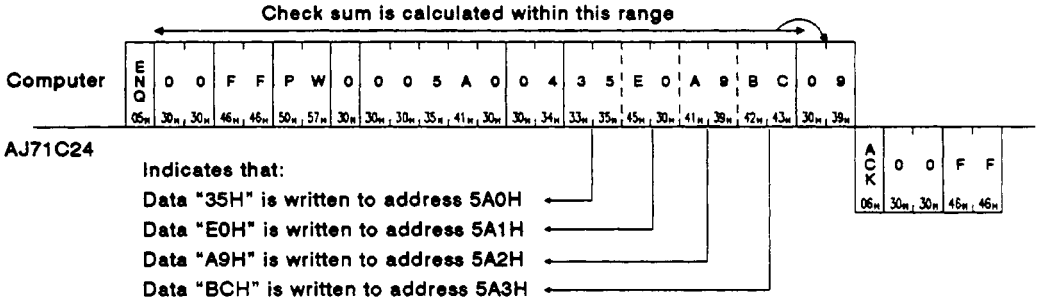
POINT

To designate the byte length, the following condition must be met:

- 1 ≤ byte length ≤ 128

Designation Example

To write 4-byte data to parameter memory addresses 5A0H to 5A3H of the PC CPU in station "0". (Message wait time is 0 msec)

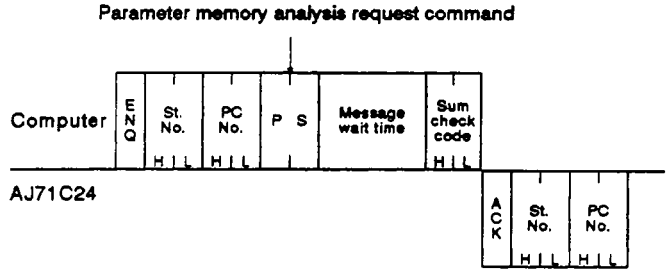

Check sum is calculated within this range
Computer
ENQ 0 0 F F P W 0 0 0 5 A 0 0 4 3 5 E 0 A 9 B C 0 9
05H 30H 30H 46H 46H 50H 57H 30H 30H 30H 35H 41H 30H 30H 34H 33H 35H 45H 30H 41H 39H 42H 43H 30H 39H
AJ71C24
ACK 0 0 F F
06H 30H 30H 46H 46H
Indicates that:
Data "35H" is written to address 5A0H
Data "E0H" is written to address 5A1H
Data "A9H" is written to address 5A2H
Data "BCH" is written to address 5A3H

(4) Parameter memory analysis request (ACPU common command)

Designation Method

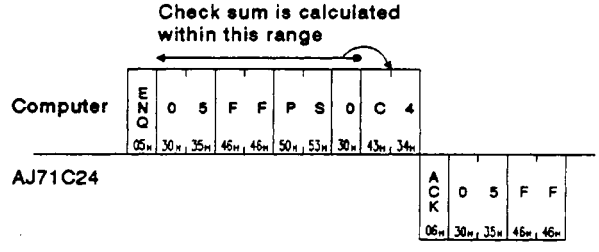
St. No. : Station number

Designation in protocol 1 is shown below.



Designation Example

To request parameter memory analysis after writing parameter to the PC CPU in station number "5". (Message wait time is 0 msec)


Check sum is calculated within this range
Computer
ENQ 0 5 F F P S 0 C 4
05H 30H, 35H 46H, 46H 50H, 53H 30H 43H, 34H
AJ71C24
ACK 0 5 F F
06H 30H, 35H 46H, 46H

8.12.4 Sequence program read/write

(1) Commands and step allocation

(a) ACPU common commands

Item			Command		Processing	Number of Points Processed per Communication	PC CPU State		
			Symbol	ASCII Code			During STOP	During RUN	
								SW22 ON	SW22 OFF
Batch read	Main	Except T/C set value	MR	4DH, 52H	Reads main sequence program.	64 steps	o	o	o
		T/C set value			Reads T/C set values used in main sequence programs.	64 points			
	Sub	Except T/C set value	SR	53H, 52H	Reads subsequence program.	64 steps	o	o	o
		T/C set value			Reads T/C set values used in subsequence programs.	64 points			
Batch write	Main	Except T/C set value	MW	4DH, 57H	Writes main sequence program.	64 steps	o	o*	x
		T/C set value			Writes T/C set values used in main sequence programs.	64 points	o	o	x
	Sub	Except T/C set value	SW	53H, 57H	Writes subsequence program.	64 steps	o	o*	x
		T/C set value			Writes T/C set values used in subsequence programs.	64 points	o	o	x

Note : o..... Executable
x..... Not executable

- Writing during a program run may executed out if all the following conditions are met:

1) The PC CPU is A3, A3N, A3H, A3M, A73, or A3A.

2) The program is not the currently running program (indicates a subprogram called by the main program, if the main program is being run).

3) The PC CPU special relay is in the following state:

i) M9050 (signal flow conversion contact).....OFF (A3CPU only)

ii) M9051 (CHG instruction disable).....ON

POINT

When reading or writing the timer/counter setting values using the sequence program read/write command, range designations of T0 to T255 or C0 to C255 are possible.

Extended ranges of T256 to T2047 and C256 to C1023 for AnA CPU should be used for storing the setting values; read or write the set values using the batch read/write command for devices (D, W, R) allocated by parameter setting. (see section 8.7)

(b) Designating the head address

The division between sequence programs and T/C set values, and their addresses in 4-digit ASCII are shown in the table below.

Example:

To read the set values T0 to T63

Head address = FE00H Command = MR

Sequence Program	Designated Step for Protocol
T0 set value T1 set value to T255 set value	FE00H FE01H to FEFFH
C0 set value C1 set value to C255 set value	FF00H FF01H to FFFFH
Step 0 Step 1 to Step 30718 (30K)	0000H 0001H to 77FEH

Calculation of designated step

Timer : Tm = FE00H + n

Counter : Cm = FF00H + n

where, m = device number

n = hexadecimal value of device number

(c) Meaning of T/C set values

T/C set values are stored as hexadecimal values as shown in the table below.

When rewriting the PC CPU set values from the computer via the AJ71C24, designate the set value in 4-digit ASCII.

Example:

Data designated to change T10 setting value K10 to K20.....0014H

Data designated to change T11 setting value D30 to D10.....800AH

Ladder Example in Program	Setting in Program	Setting in Protocol
K[][][][][] T[][][]	K0 K1 to K9	0000H 0001H to 0009H
K[][][][][] C[][][]	K10 to K32767	000AH to 7FFFH
D[][][][][] T[][][]	D0 D1 D2	8000H 8002H 8004H
D[][][][][] C[][][]	to D1023	to 87FEH

Calculation of protocol setting value

Km = 0000H + n

Dm = 8000H + 2n

where, m = device number

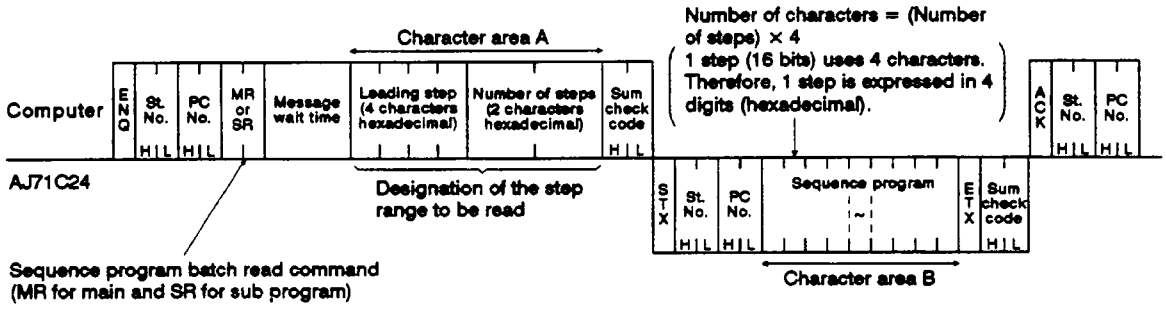
n = hexadecimal value of device number

(2) Sequence program batch read (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.


Character area A
Number of characters = (Number of steps) × 4
1 step (16 bits) uses 4 characters. Therefore, 1 step is expressed in 4 digits (hexadecimal).
Computer
ENQ
St. No.
PC No.
MR or SR
Message wait time
Leading step (4 characters hexadecimal)
Number of steps (2 characters hexadecimal)
Sum check code
ACK
AJ71C24
Designation of the step range to be read
STX
Sequence program
ETX
Character area B
Sequence program batch read command
(MR for main and SR for sub program)

POINTS

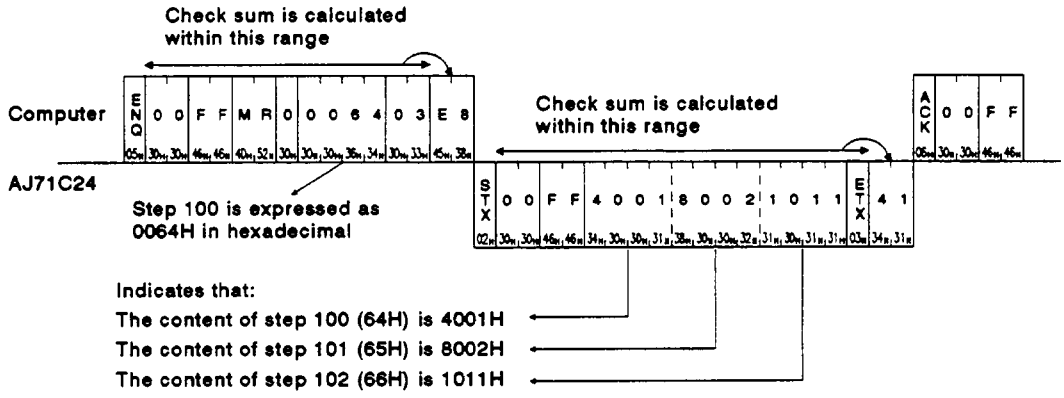
(1) To designate the number of steps, the following condition must be met:

- 1 ≤ number of steps ≤ 64

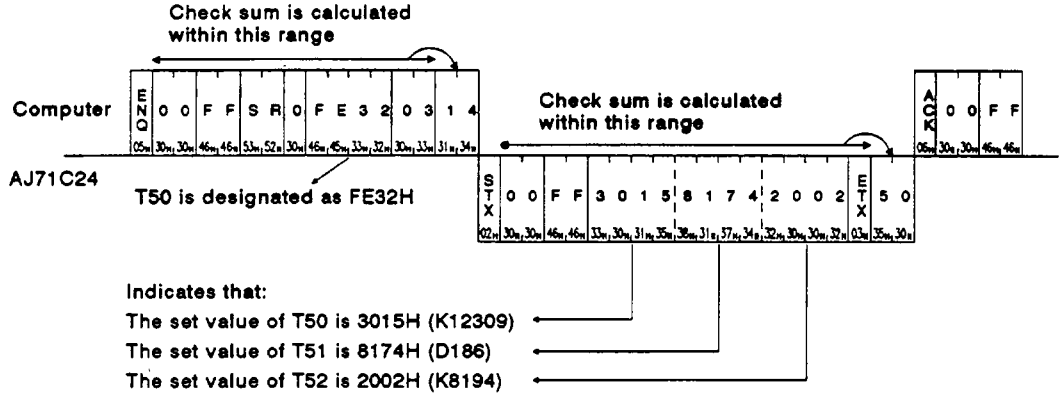
(2) Timers, counters, and a sequence program cannot be used in combination. Only one of these may be set.

Designation Examples

Example 1:
To read 3 steps: step 100 to step 102 of the main sequence program of the PC CPU in station number "0". (Message wait time is 0 msec)


Check sum is calculated within this range
Computer
ENQ 0 0 F F M R 0 0 0 6 4 0 3 E 8
Check sum is calculated within this range
ACK 0 0 F F
AJ71C24
Step 100 is expressed as 0064H in hexadecimal
STX 0 0 F F 4 0 0 1 8 0 0 2 1 0 1 1 ETX 4 1
Indicates that:
The content of step 100 (64H) is 4001H
The content of step 101 (65H) is 8002H
The content of step 102 (66H) is 1011H

Example 2:
To read set values at 3 points: T50 to T52 of the subsequence program of the PC CPU in station number "0". (Message wait time is 0 msec)

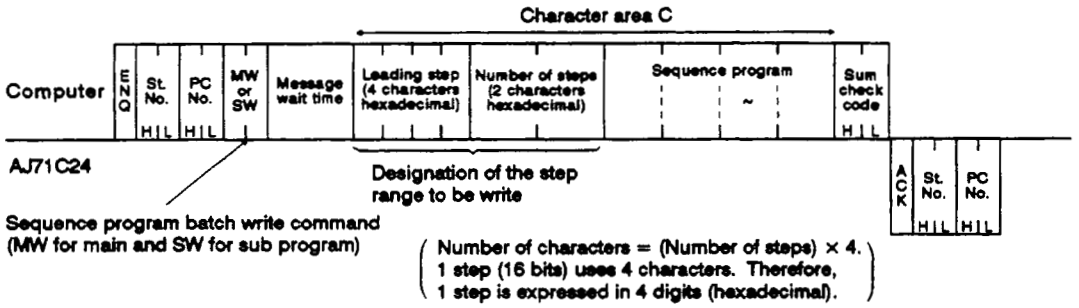

Check sum is calculated within this range
Computer
ENQ 0 0 F F S R 0 F E 3 2 0 3 1 4
Check sum is calculated within this range
ACK 0 0 F F
AJ71C24
T50 is designated as FE32H
STX 0 0 F F 3 0 1 5 8 1 7 4 2 0 0 2 ETX 5 0
Indicates that:
The set value of T50 is 3015H (K12309)
The set value of T51 is 8174H (D186)
The set value of T52 is 2002H (K8194)

(3) Sequence program batch write (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.


Character area C
Computer
ENQ
St. No.
PC No.
MW or SW
Message wait time
Leading step (4 characters hexadecimal)
Number of steps (2 characters hexadecimal)
Sequence program
Sum check code
H L
AJ71C24
Designation of the step range to be write
ACK
St. No.
PC No.
Sequence program batch write command (MW for main and SW for sub program)
Number of characters = (Number of steps) × 4.
1 step (16 bits) uses 4 characters. Therefore,
1 step is expressed in 4 digits (hexadecimal).

POINTS

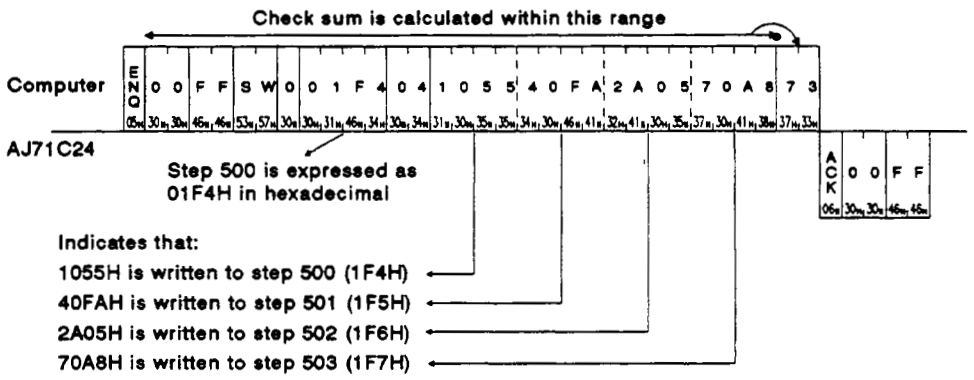
(1) To designate the number of steps, the following condition must be met:

- 1 ≤ number of steps ≤ 64

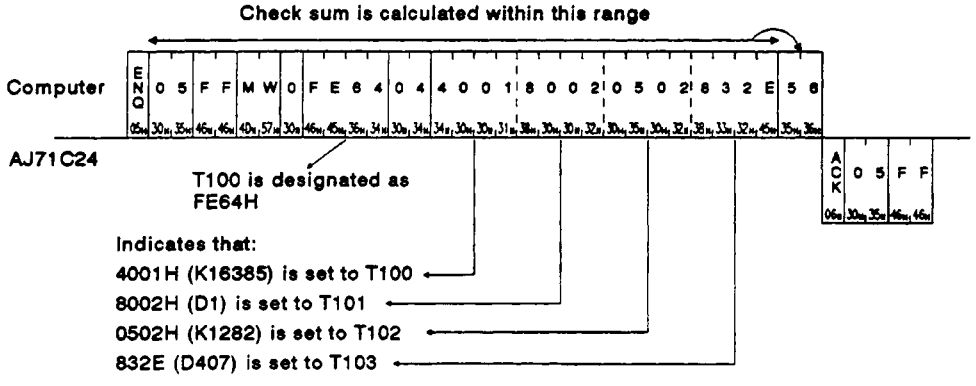
(2) Timers, counters, and the sequence program cannot be used in combination. Only one of these may be set.

Designation Examples

Example 1:
To write a program to 4 steps: step 500 to step 503 of the subsequence program of the PC CPU in station number "0". (Message wait time is 0 msec)


Check sum is calculated within this range
Computer
ENQ 0 0 F F S W 0 0 1 F 4 0 4 1 0 5 5 4 0 F A 2 A 0 5 7 0 A 8 7 3
AJ71C24
Step 500 is expressed as 01F4H in hexadecimal
ACK 0 0 F F
Indicates that:
1055H is written to step 500 (1F4H)
40FAH is written to step 501 (1F5H)
2A05H is written to step 502 (1F6H)
70A8H is written to step 503 (1F7H)

Example 2:
To write set values to 4 points: T100 to T103 of the main sequence program of the PC CPU in station number "5". (Message wait time is 0 msec)


Check sum is calculated within this range
Computer
ENQ 0 5 F F M W 0 F E 6 4 0 4 4 0 0 1 8 0 0 2 0 5 0 2 8 3 2 E 5 8
AJ71C24
T100 is designated as FE64H
ACK 0 5 F F
Indicates that:
4001H (K16385) is set to T100
8002H (D1) is set to T101
0502H (K1282) is set to T102
832E (D407) is set to T103

8.12.5 Microcomputer program read/write

(1) Commands and addresses

Commands and program addresses to read and write microcomputer programs are explained below:

(a) ACPU common commands

Item		Command		Processing	Number of Points Processed per Communication	State of PC CPU		
		Symbol	ASCII Code			During STOP	During RUN	
							SW22 ON	SW22 OFF
Batch read	Main	UR	55H, 52H	Reads microcomputer main programs.	128 bytes	o	o	o
	Sub	VR	56H, 52H	Reads microcomputer subprograms.				
Batch write	Main	UW	55H, 57H	Writes microcomputer main programs.	128 bytes	o	o*	x
	Sub	VW	56H, 57H	Writes microcomputer subprograms.				

Note : o.....Executable
x.....Not executable

* Writing during a program run may be executed if all the following conditions are met:

1) The PC CPU is A3, A3N, A3H, A3M or A73.

2) The program is not currently running program (indicates a sub-program called by the main program, if the main program is being run).

3) The PC CPU special relay is in the following state:

M9050 (signal flow conversion contact) : OFF (A3CPU only)

M9051 (CHG instruction disable) : ON

(b) Microcomputer program address

Microcomputer addresses are designated in the protocol as follows:

1) The range of addresses that can be set for each PC CPU is shown in the table on the next page.

CPU Model	Microcomputer Program Capacity	Microcomputer Program Addresses
A0J2HCPU A1SCPU A2CCPU	Max. 14K bytes	0000H to 37FEH
A1CPU A1NCPU	Max. 10K bytes	0000H to 27FEH
A2CPU(S1) A2NCPU(S1)	Max. 26K bytes	0000H to 67FEH
A3CPU A3NCPU A3HCPU A3MCPU A73CPU	Main and sub Max. 58K bytes	0000H to E7FEH

2) Addresses are set by converting 4-digit hexadecimals into ASCII.

3) A character area error 06H occurs if the following condition is not met:

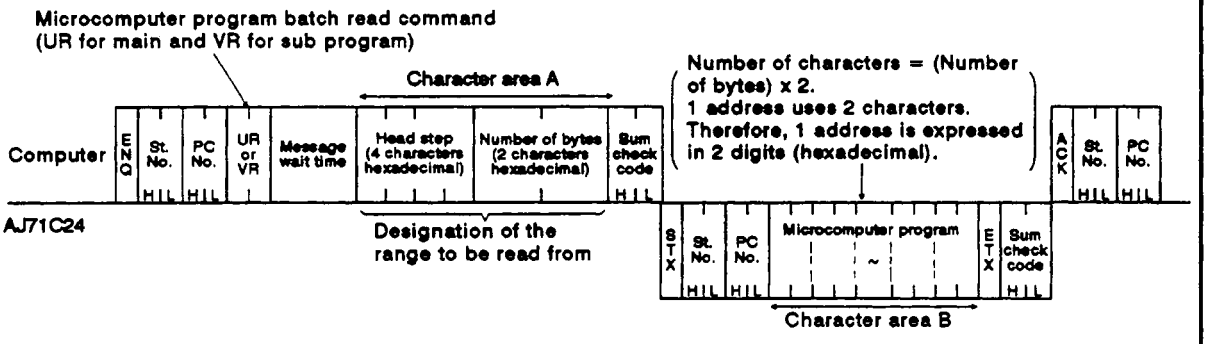
   Head address + (number of bytes) − 1 ≥ microcomputer program capacity.

(2) Microcomputer program batch read (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



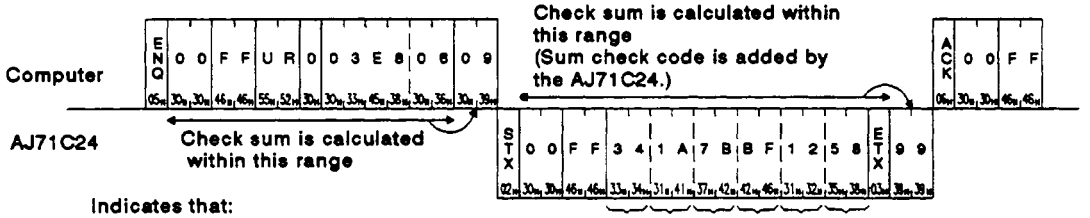
POINT

To set the number of bytes, the following conditions must be met:

- 1 ≤ number of bytes ≤ 128
- (Head address) + [(number of bytes) - 1] ≤microcomputer program capacity

Designation Example

To read 6 bytes of a microcomputer program beginning with address 03E8H (1000 in decimal) in the PC CPU of station number"0". (Message wait time is 0 msec)


Check sum is calculated within this range
(Sum check code is added by the AJ71C24.)
Computer
ENQ 0 0 F F U R 0 0 3 E 8 0 6 0 9
ACK 0 0 F F
AJ71C24
Check sum is calculated within this range
STX 0 0 F F 3 4 1 A 7 B B F 1 2 5 8 ETX 9 9
(1) (2) (3) (4) (5) (6)

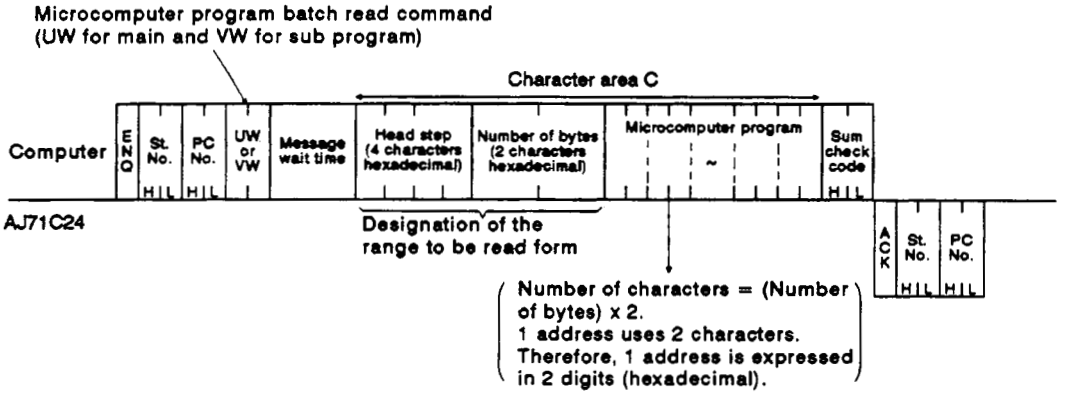
Indicates that:
(1) the contents of address 03E8H is 34H,
(2) the contents of address 03E9H is 1AH,
(3) the contents of address 03EAH is 7BH,
(4) the contents of address 03EBH is BFH,
(5) the contents of address 03ECH is 12H, and
(6) the contents of address 03EDH is 58H.

(3) Microcomputer program batch write (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



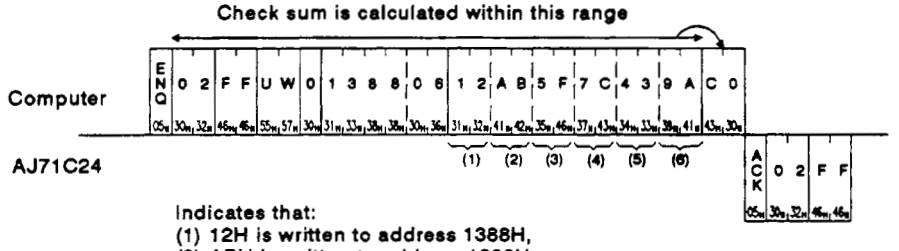
POINT

To set the number of bytes, the following conditions must be met:

- 1 ≤ number of bytes ≤ 128
- (Head address) + [(number of bytes) – 1] ≤ Microcomputer program capacity

Designation Example

To write 6 bytes of a microcomputer program to the area beginning with address 1338H (5000 in decimal) in the PC CPU of station number "2". (Message wait time is 0 msec)



Indicates that:
(1) 12H is written to address 1388H,
(2) ABH is written to address 1389H,
(3) 5FH is written to address 138AH,
(4) 7CH is written to address 138BH,
(5) 43H is written to address 138CH, and
(6) 9AH is written to address 138DH.

8.12.6 Comment memroy read/write

(1) Commands and addresses

Commands and comment data addresses to read and write comment data are explained below.

(a) ACPU common commands

Item		Command		Processing	Number of Points Processed per Communication	State of PC CPU		
		Symbol	ASCII Code			During STOP	During RUN	
							SW22 ON	SW22 OFF
Batch read	Main	KR	4BH, 52H	Reads from comment memory.	128 bytes	o	o	o
Batch write	Sub	KW	4BH, 57H	Writes to comment memory.	128 bytes	o	o	o

Note : o.....Executable
x.....Not executable

(b) Comment memory addresses

The area to store comment data is managed using relative addresses from the head address 00H.

For example, for 2K bytes of parameter comments, the range in which the addresses may be specified for the head address is 00H to 7FHH.

1) Comment memory capacity is 64K bytes

The comment data address range is determined by the parameter setting.

2) Comment memory addresses are designated in 4-digit ASCII. (0000 to FFFF)

3) A character area error 06H occurs if the following condition is not met:

Head address + designated number of bytes ≤ comment memory capacity.

POINT

It is not possible to designate a particular device or device number when reading or writing comment data.

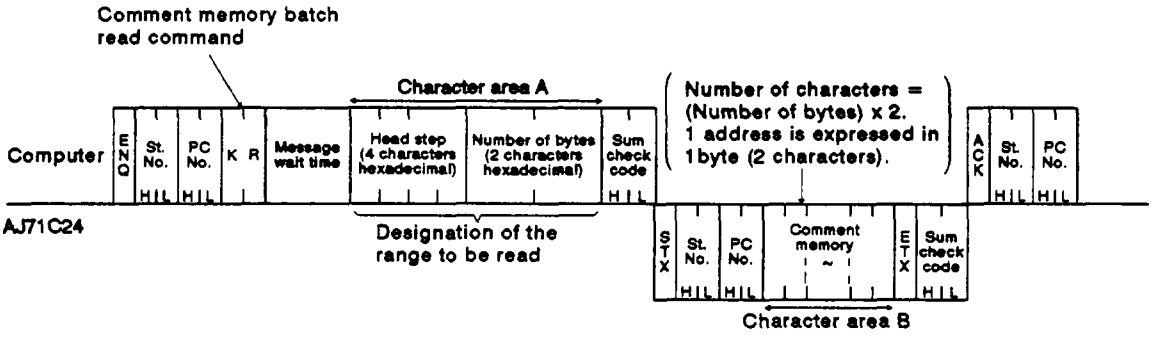
Always read or write all data from address 0H.

(2) Comment memory batch read (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



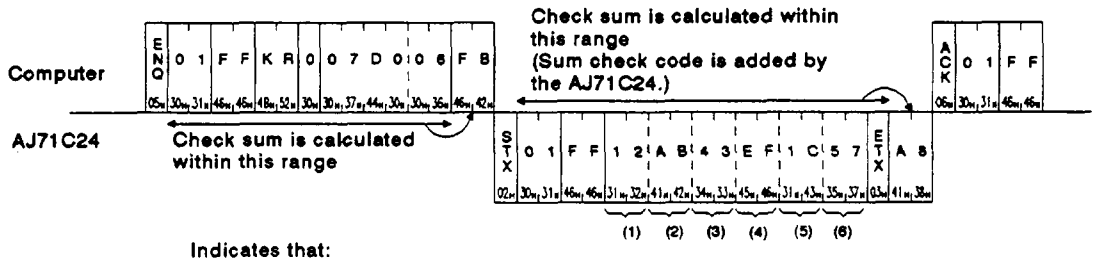
POINT

To designate the number of bytes, the following conditions must be met:

- 1 ≤ number of bytes ≤ 128
- (Head address) + [(number of bytes) - 1] ≤ Comment memory capacity

Designation Example

To read 6 bytes of comment memory data beginning with address 7D0H (2000 in decimal) in the PC CPU of station number"1". (Message wait time is 0 msec)


Computer
ENQ 0 1 F F K R 0 0 7 D 0 0 0 6 F B
Check sum is calculated within this range
Check sum is calculated within this range (Sum check code is added by the AJ71C24.)
ACK 0 1 F F
AJ71C24
STX 0 1 F F 1 2 A B 4 3 E F 1 C 5 7 ETX A 8
(1) (2) (3) (4) (5) (6)

Indicates that:
(1) the content of address 07D0H is 12H,
(2) the content of address 07D1H is ABH,
(3) the content of address 07D2H is 43H,
(4) the content of address 07D3H is EFH,
(5) the content of address 07D4H is 1CH, and
(6) the content of address 07D5H is 57H.

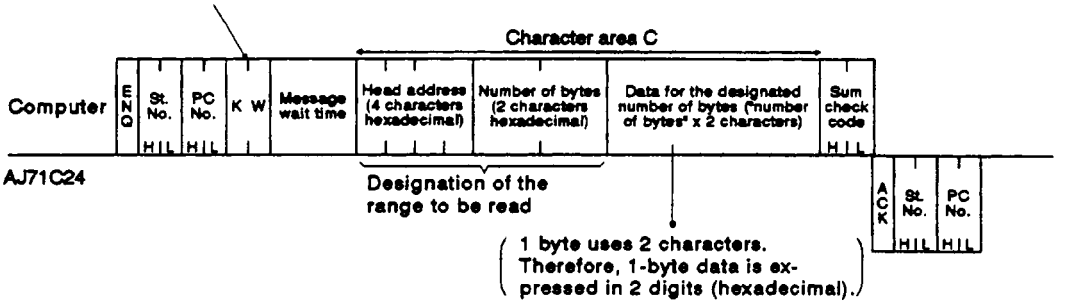
(3) Comment memory batch write (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.

Comment memory batch read command



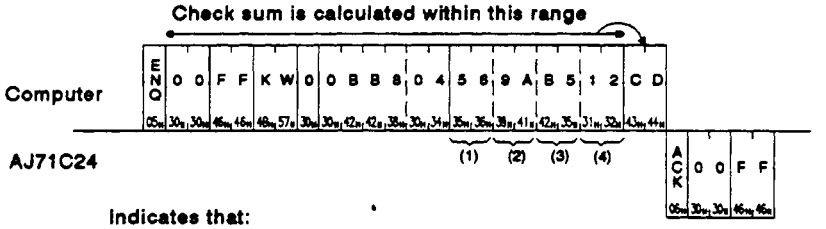
POINT

To set the number of bytes, the following conditions must be met:

- 1 ≤ number of bytes ≤ 128
- (Head address) + [(number of bytes) – 1] ≤ Comment memory capacity

Designation Example

To write 4 bytes of comments to the area beginning with address 0BB8H (3000 in decimal) in the PC CPU of station number "0". (Message wait time is 0 msec)



Indicates that:
(1) 56H is written to address 0BB8H,
(2) 9AH is written to address 0BB9H,
(3) B5H is written to address 0BBAH, and
(4) 12H is written to address 0BBBH.

8.12.7 Extension comment memory read/write

(1) Commands and addresses

(a) AnACPU dedicated commands

Item	Command		Processing	Number of Points Processed Per Communication	State of PC CPU		
	Symbol	ASCII Code			During STOP	During RUN	
						SW22 ON	SW22 OFF
Batch read	DR	44H, 52H	Reads from the extension comment memory.	128 bytes	o	o	o
Batch write	DW	44H, 57H	Writes to the extension comment memory.	128 bytes	o	o	x

Note : o.....Executable
x.....Not executable

(b) Extension comment memory addresses

The extension comment data storage area is managed in relative addresses with the head address 00H.

For example, the range that can be set to the head address for an extension comment memory of 3K bytes is 00H to BFFH.

1) The maximum extension comment memory area is 63K bytes.

   The address range for the extension comment data is determined in accordance with the paraemter set capacity.

2) Designation of the extension comment memory address is made by converting 5-digit hexadecimal into ASCII code (00000 to 0FFFF).

3) A character error "06H" occurs if the extension comment memory capacity is not equal to or greater than [head address + (set number of bytes – 1)].

POINT

Reading or writing extension comment data by designating specific devices or device numbers is not possible.

Always read or write extension comment data beginning with address 0H.

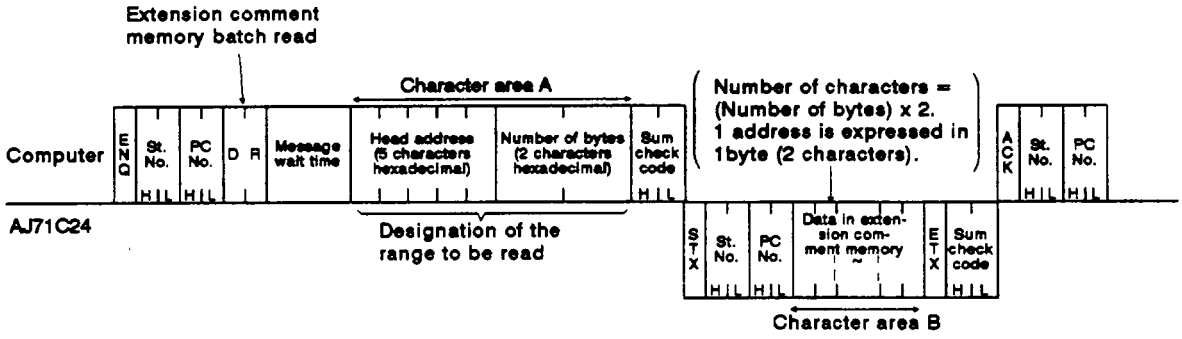
(2) Extension comment memory batch read

Batch read of the extension comment memory using an AnACPU dedicated command is shown below.

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



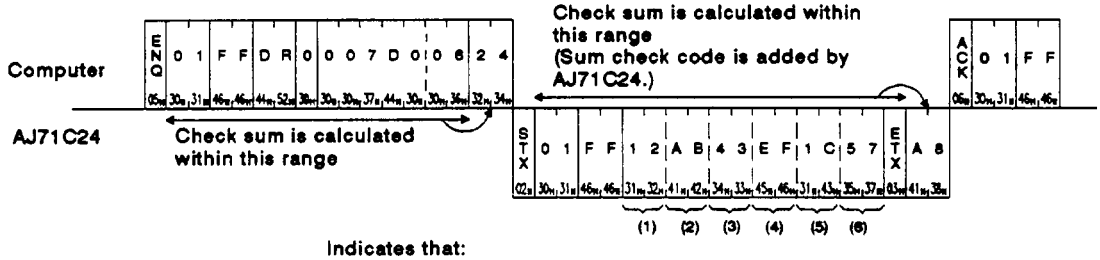
POINT

To set the number of bytes, the following conditions must be met:

- 1 ≤ number of bytes ≤ 128
- (Head address) + [(number of bytes) – 1] ≤ extension coment memory capacity

Designation Example

To read 6 bytes of data from the extension comment memory beginning with 7D0H (2000 in decimal) in station "1". (Message wait time is 0 msec)


Check sum is calculated within this range (Sum check code is added by AJ71C24.)
Computer
AJ71C24
Check sum is calculated within this range
(1) (2) (3) (4) (5) (6)

Indicates that:
(1) the content of address 07D0H is 12H,
(2) the content of address 07D1H is ABH,
(3) the content of address 07D2H is 43H,
(4) the content of address 07D3H is EFH,
(5) the content of address 07D4H is 1CH, and
(6) the content of address 07D5H is 57H.

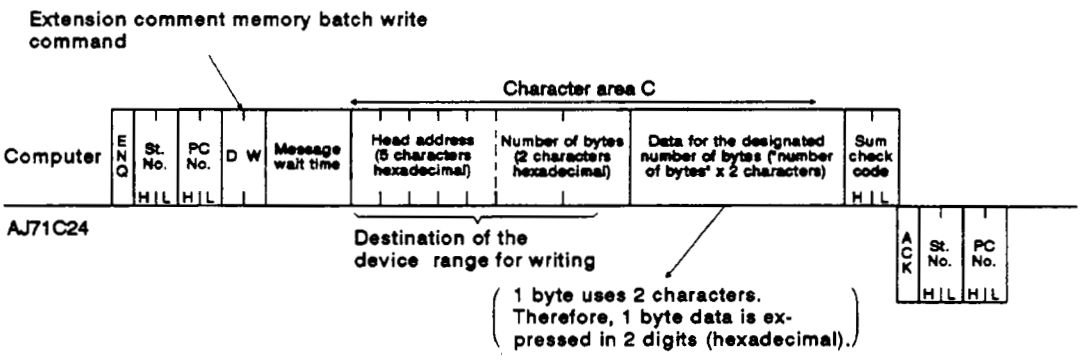
(3) Extension comment memory batch write

Batch write of data to the extension comment memory using an AnACPU dedicated command is shown below.

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.


Extension comment memory batch write command
Character area C
Computer
ENQ
St. No.
PC No.
D W
Message wait time
Head address (5 characters hexadecimal)
Number of bytes (2 characters hexadecimal)
Data for the designated number of bytes (*number of bytes* x 2 characters)
Sum check code
H L
AJ71C24
ACK
Destination of the device range for writing
1 byte uses 2 characters. Therefore, 1 byte data is expressed in 2 digits (hexadecimal).

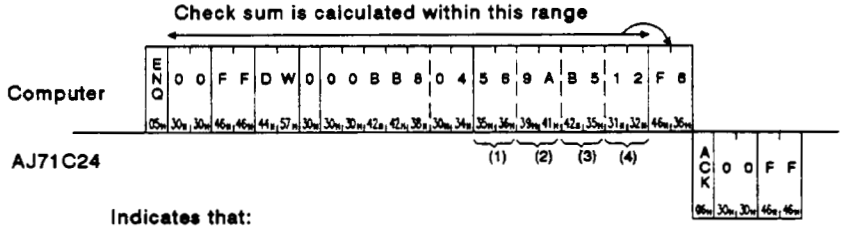
POINT

To set the number of bytes, the following conditions must be met:

- 1 ≤ number of bytes ≤ 128
- (Head address) + [(number of bytes) – 1] ≤ extension comment memory capacity

Designation Example

To write 4 bytes of extension comment to the extension comment memory area beginning with 0BB8H (3000 in decimal) in station number "0". (Message wait time is 0 msec)



Indicates that:
(1) 56H is written to address 0BB8H,
(2) 9AH is written to address 0BB9H,
(3) B5H is written to address 0BBAH, and
(4) 12H is written to address 0BBBH.

8.13 Global Function

The global function is used to switch the Xn2 input signal at each AJ71C24 in all stations connected to the computer by the multidrop link.

This function is used for emergency instructions simultaneous start, etc., to the PC CPU.

8.13.1 Commands and control

(1) ACPU common commands

Item	Command		Processing	State of PC CPU		
	Symbol	ASCII Code		During STOP	During RUN	
					SW22 ON	SW22 OFF
Global	GW	47H, 57H	Turns ON/OFF Xn2 of the AJ71C24 loaded in each PC CPU system.	o	o	o

Note : o.....Executable

(2) Control

This function switches the Xn2 input signal at each AJ71C24 in all stations linked to the computer.

(a) Xn2 is determined by the I/O addresses of the AJ71C24s.

Example: If the I/O addresses are 90 to AF, Xn2 is X92.

(b) Designate the station number in the control protocol as FFH.

Designating a number other than FFH causes the Xn2 of the AJ71C24 at the designated station number to turn ON/OFF.

(c) This function is a command from the computer. A reply is not given by the AJ71C24.

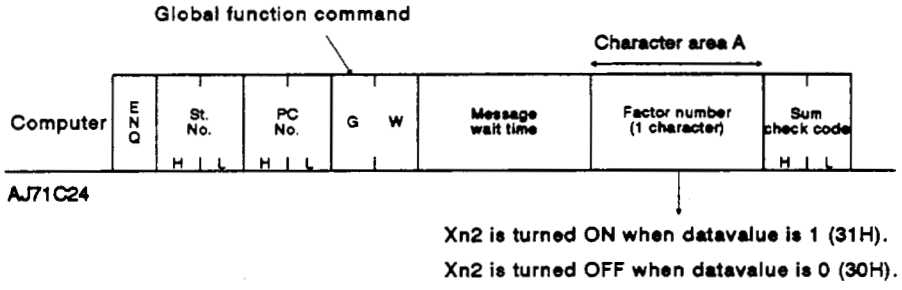
(d) When the power supply to a PC CPU is turned OFF, the PC CPU is reset, or the mode of the AJ71C24 is switched, the Xn2 signal at all stations is turned OFF and the global function processing request is cleared.

8.13.2 Setting the global function (ACPU common command)

Designation Method

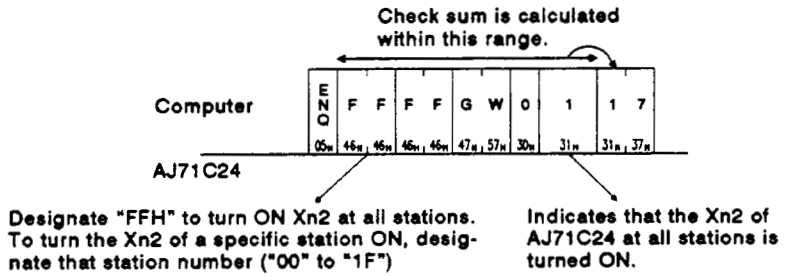
St. No. : Station Number

Designation in protocol 1 is shown below.



Designation Example

To turn the Xn2 of AJ71C24 ON at all stations. (Message wait time is 0 msec.)

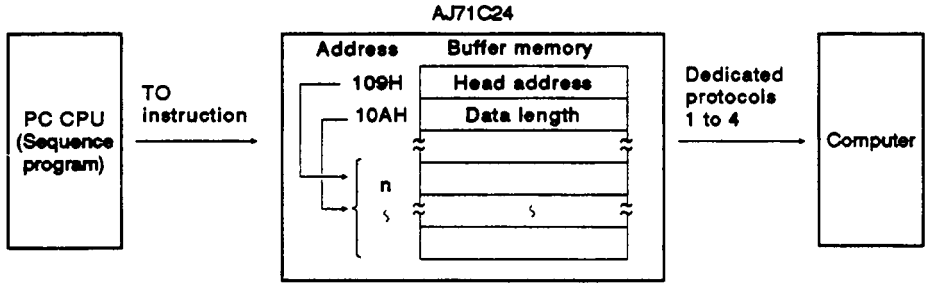

Check sum is calculated within this range.
Computer
ENQ
F F F F G W 0 1 1 7
05H 46H, 46H 46H, 46H 47H, 57H 30H 31H 31H, 37H
AJ71C24
Designate "FFH" to turn ON Xn2 at all stations. To turn the Xn2 of a specific station ON, designate that station number ("00" to "1F")
Indicates that the Xn2 of AJ71C24 at all stations is turned ON.

8.14 On-demand Function

The on-demand function is used when the PC CPU has data to transmit to the computer. In this case, the PC CPU specifies the buffer memory area in which the data to be transmitted is stored and then starts transmission.

During data transmission between the computer and PC CPU using dedicated protocols 1 to 4, communications is normally initiated by the computer.

If the PC CPU has emergency data to transmit to the computer, the on-demand function is used.



POINT

This function is available only when there is a 1:1 ratio of computers to PC CPUs.

8.14.1 On-demand handshake signal and buffer memory

(1) On-demand handshake signal

The on-demand handshake signal turns ON when the PC CPU transmits a data send request to the computer to start transmission, and turns OFF when transmission of the data specified by the AJ71C24 is completed. It acts as an interlock to prevent on-demand requests being made simultaneously.

Handshake Signal	Description	Signal Turned ON/OFF by
Xn3*	During execution of on-demand function ON : transmission underway OFF : transmission completed	AJ71C24

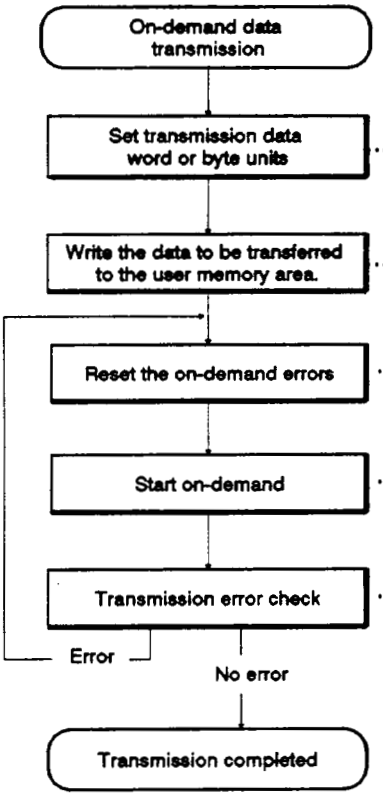
• "n" in Xn3 is determined by the slot location of the AJ71C24.

(2) Buffer memory used by the on-demand function

Address	Name	Description
109H	Area to specify head address in on-demand buffer memory	The head address of the data stored in the buffer memory to be transmitted by the on-demand function is specified by the TO instruction of the Sequence program.
10AH	Area to specify data length	The length of the data to be transmitted by the on-demand function is specified by the PC CPU TO instruction of the sequence program.
10CH	On-demand error storage area	The AJ71C24 writes a "1" to this address if a transmission error occurs during on-demand data transmission. 0 : No error 1 : Error

8.14.2 On-demand function control procedure

(1) PC CPU control procedure



Check (and if necessary change) the contents of buffer memory address 103H. See Examples 1 and 2 in Section 8.14.3 for transmission data formats when word or byte units are selected.

Write to buffer memory address 0H to FFH or 120H to 7FFH (*1)

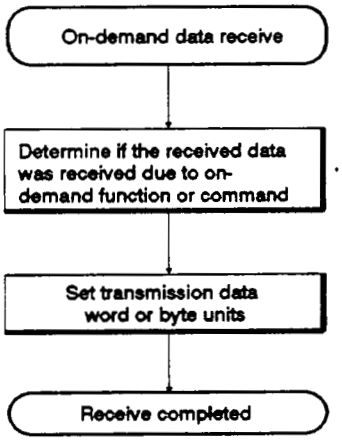
Clear the on-demand buffer memory address 10CH. (Start is disabled if the contents of this address are "1".)

Write the head address where the data is stored to buffer memory address 109H and the data length to address 10AH.
When a data transmission request from the PC CPU is sent to the computer, the Xn3 signal goes ON.
When data transmission is completed, the Xn3 signal goes OFF.

If "1" is written to buffer memory address 10CH, an error occurs and the data is not transmitted.

*1
If data communications is executed at the same time in either the no-protocol mode or the bidirectional mode, the area must not overlap with the following area.
- No-protocol send area (bidirectional send area)
- No-protocol receive area (bidirectional receive area)

(2) Computer control procedure

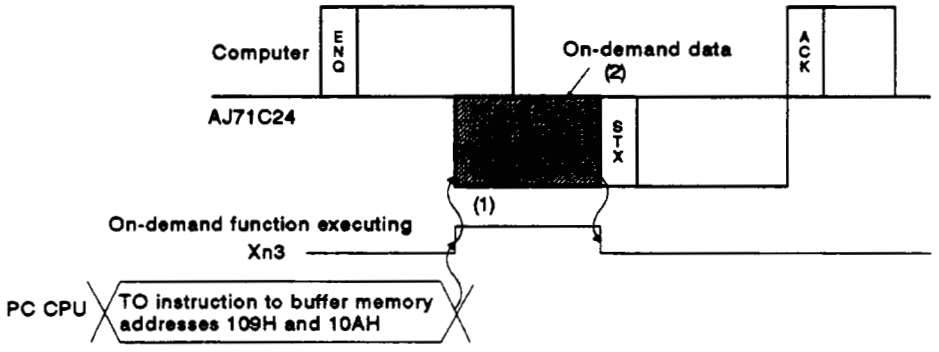

On-demand data receive
Determine if the received data was received due to on-demand function or command
Set transmission data word or byte units
Receive completed

The AJ71C24 appends "FE" as the PC CPU number. Process data as on-demand data only if the PC CPU number of the received data is FE.

(3) On-demand request processing timing chart

(a) Full-duplex communications

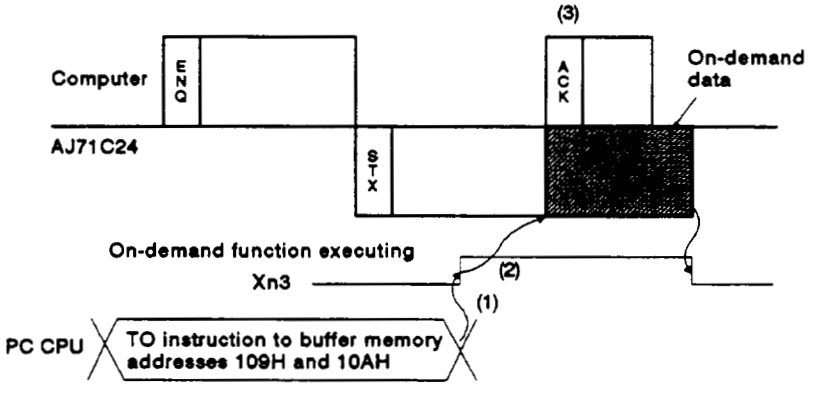
Computer is transmitting data



1) The on-demand function executing signal (Xn3) turns ON immediately and , the on-demand data is transmitted when the on-demand request is made.

2) Transmission of response data (beginning with STX) to the command data (beginning with ENQ) is suspended until the completion of on-demand data transmission.

Computer is receiving data



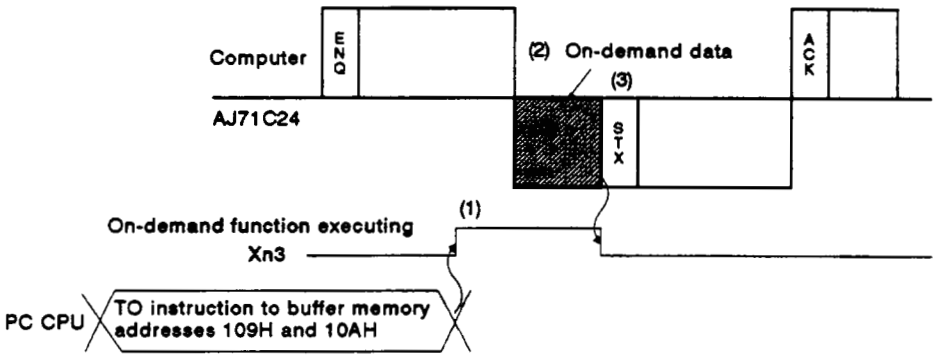
1) The on-demand function executing signal (Xn3) turns ON immediately when the on-demand request is made.

2) Transmission of the on-demand data is suspended until the completion of the response data (beginning with STX) to the command data (beginning with ENQ).

3) Transmission of the response data (beginning with ACK) from the computer in response to the response data (beginning with STX) from the AJ71C24 is possible while the on-demand data is received.

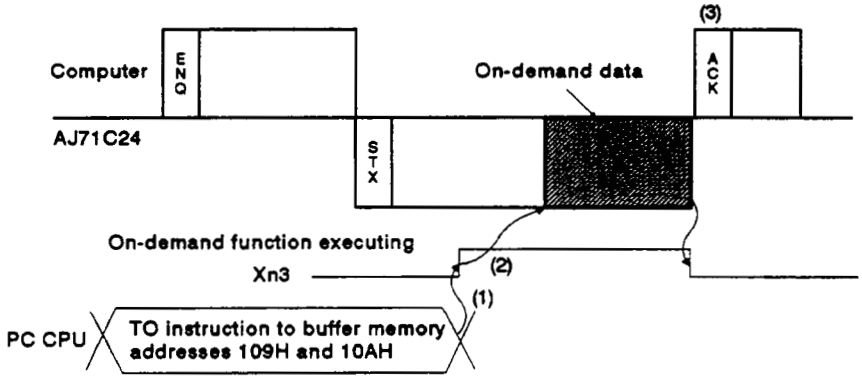
(b) Half-duplex communications

Computer is transmitting data



1) The on-demand function executing signal (Xn3) turns on immediately when the on-demand request is made.
2) Transmission of on-demand data is suspended until the completion of command data receive (beginning with ENQ) from the computer.
3) Transmission of response data (beginning with STX) to the command data (beginning with ENQ) is suspended until the completion of on-demand data transmission.

Computer is receiving data

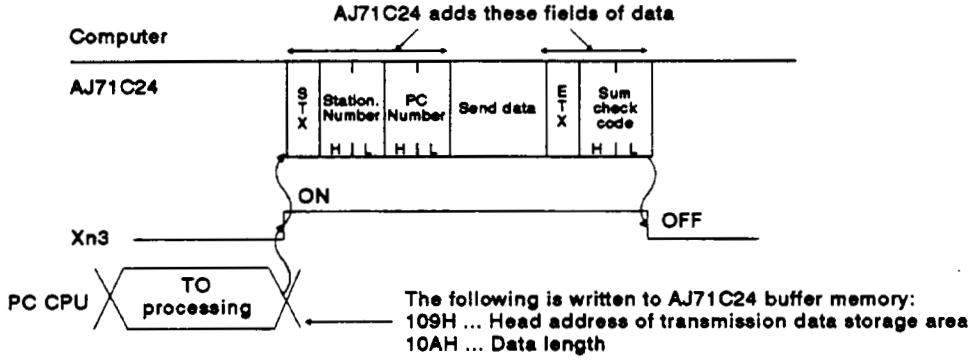


1) The on-demand function executing signal (Xn3) turns ON immediately when the on-demand request is made.
2) Transmission of the on-demand data is suspended unil the completion of the response data (beginning with STX) to the command data (beginning with ENQ).
3) Transmission of the response data (beginning with ACK) from the computer in response to the response data (beginning with STX) from the AJ71C24 should be made after the completion of on-demand data receive.

8.14.3 On-demand function designation

Designation Method

Designation in protocol 1 is shown below.



POINTS

(1) Buffer memory area 100H to 11FH is the special applications area.

Do not use this area to store the data to be transmitted with the on-demand function.

(2) Data length setting range must meet the following criteria:

- When the buffer memory area of 0H to FFH is used:

  (Head address) + [(data length) – 1] ≤ FFH

- When the buffer memory area of 120H to 7FFH is used:

  (Head address) + [(data length) – 1] ≤ 7FFH

(3) The AJ71C24 appends "FE" as the PC CPU number.

(4) The block number is "00H" when protocol 2 is used.

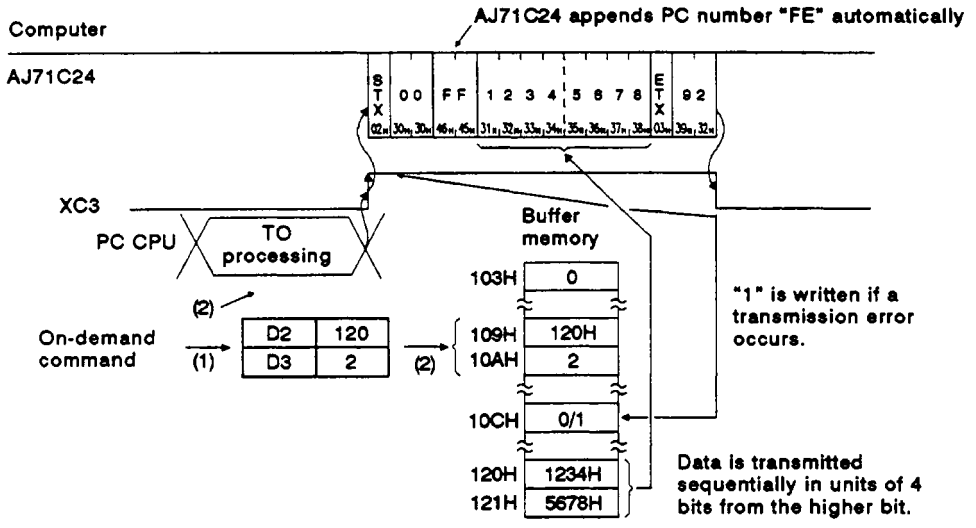
IMPORTANT

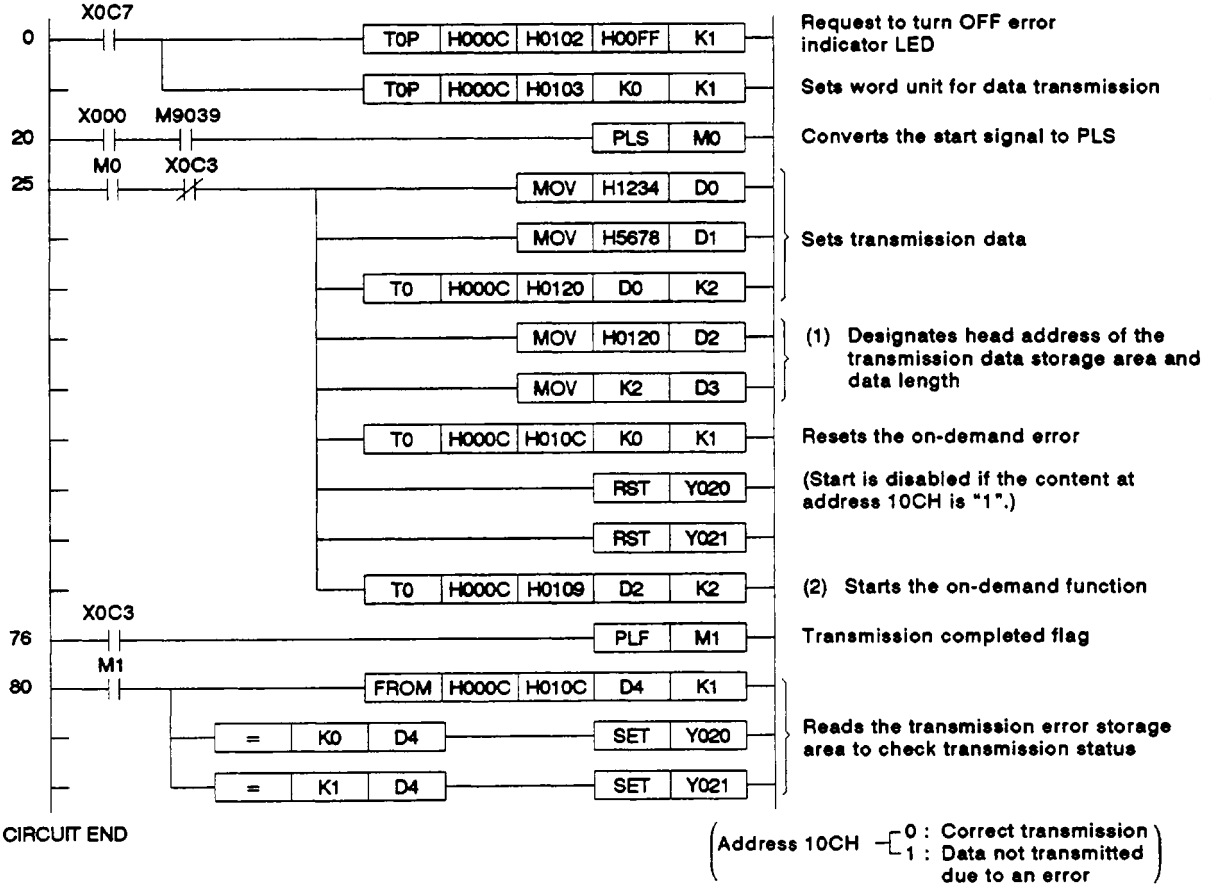
The on-demand function may be used only when the system configuration is a 1:1 ratio of computers to PC CPUs.

If the on-demand function is used in a multidrop link system of 1:n, 2:n, or m:n ratios, communications data in control protocols 1 to 4 and on-demand transmission data will be destroyed and correct data transmission is precluded.

Designation Examples

Example 1:
To start transmission of data, stored in buffer memory at addresses 120H and 121H, by the sequence program. (Station number is "0", AJ71C24 I/O addresses are C0 to DF, transmission data is designated in word units.)

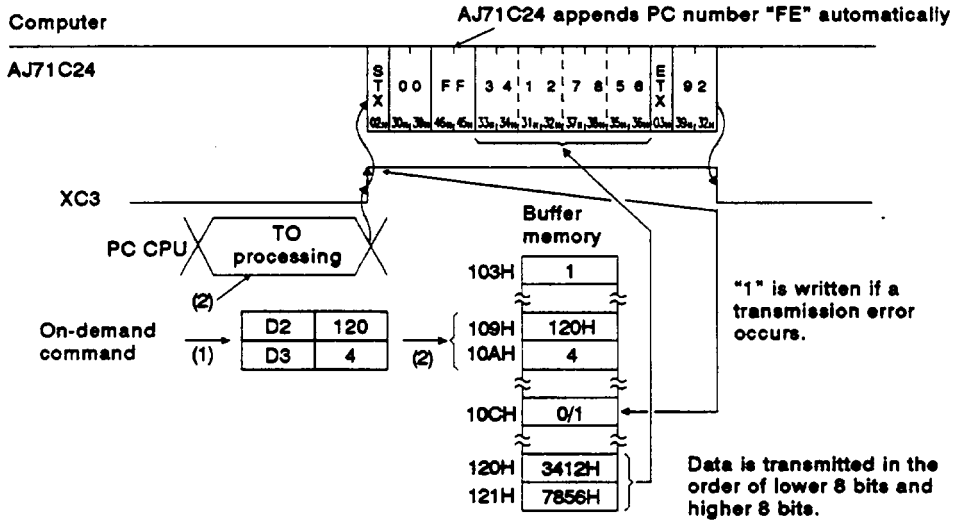


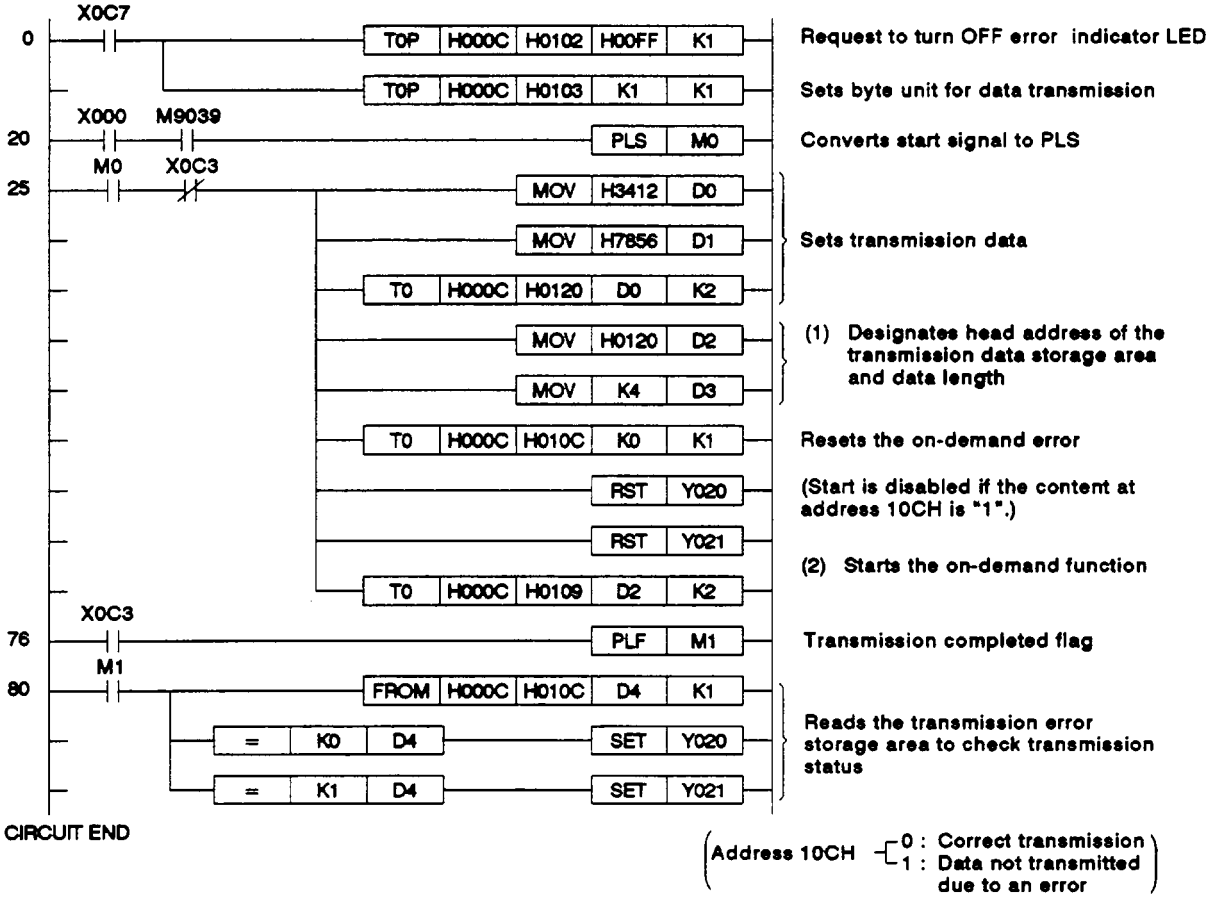

0 X0C7 TOP H000C H0102 H00FF K1
Request to turn OFF error indicator LED
TOP H000C H0103 K0 K1
Sets word unit for data transmission
20 X000 M9039 PLS M0
Converts the start signal to PLS
25 M0 X0C3 MOV H1234 D0
MOV H5678 D1
Sets transmission data
TO H000C H0120 D0 K2
MOV H0120 D2
MOV K2 D3
(1) Designates head address of the transmission data storage area and data length
TO H000C H010C K0 K1
Resets the on-demand error
RST Y020
(Start is disabled if the content at address 10CH is "1".)
RST Y021
TO H000C H0109 D2 K2
(2) Starts the on-demand function
76 X0C3 PLF M1
Transmission completed flag
80 M1 FROM H000C H010C D4 K1
= K0 D4 SET Y020
= K1 D4 SET Y021
Reads the transmission error storage area to check transmission status
CIRCUIT END
Address 10CH 0 : Correct transmission
1 : Data not transmitted due to an error

Designation Examples

Example 2:

To start transmission of data, stored in buffer memory at addresses 120H and 121H, by the sequence program. (Station number is "0", AJ71C24 I/O addresses are 80 to 9F, transmission data is designated in byte units.)





8.15 Loopback Test

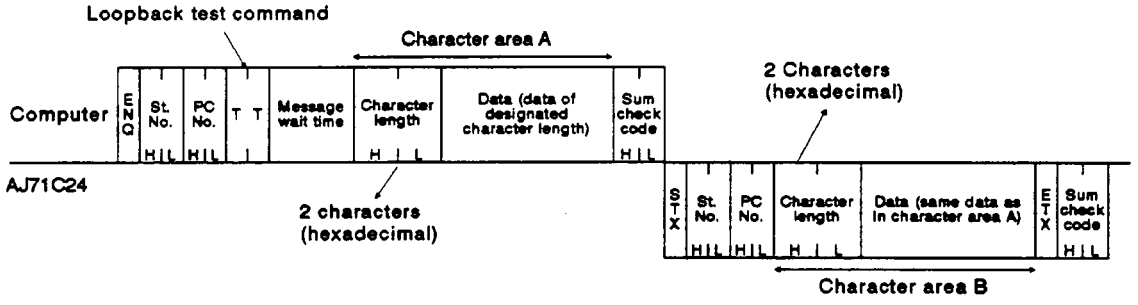
(1) ACPU common command

Item	Command		Processing	Number of Points Processed per Communication	State of PC CPU		
	Symbol	ASCII Code			During STOP	During RUN	
						SW22 ON	SW22 OFF
Loopback test	TT	54H, 54H	Echoes back the characters to the computer as they are received	254 characters	o	o	o

(2) Designating the loopback test

Designation Method

Designation in protocol 1 is shown below.



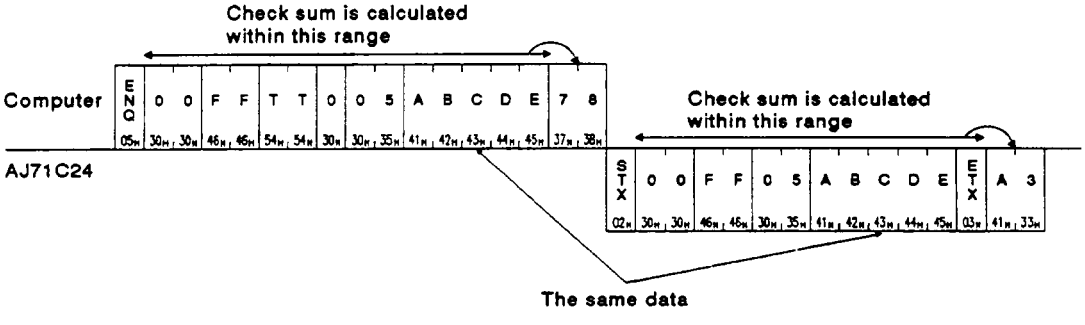
POINT

To set the characer length, the following condition must be met:

- 1 ≤ character length ≤ 254

Designation Example

To execute the loopback test with the "ABCDE" at station number "0". (Message wait time is 0 msec.)


Check sum is calculated within this range
Computer
ENQ 0 0 F F T T 0 0 5 A B C D E 7 8
05H 30H 30H 46H 46H 54H 54H 30H 30H 35H 41H 42H 43H 44H 45H 37H 38H
AJ71C24
Check sum is calculated within this range
STX 0 0 F F 0 5 A B C D E ETX A 3
02H 30H 30H 46H 46H 30H 35H 41H 42H 43H 44H 45H 03H 41H 33H
The same data

9. COMMUNICATIONS WITH A COMPUTER IN THE NO-PROTOCOL MODE

Read this section if the RS-422 and RS-232C interfaces are used with the dedicated protocol in the no-protocol mode by (a) setting the AJ71C24 mode setting switch at any position from 1 to 8, or (b) using the mode switching function to set any mode number from 1 to 9.

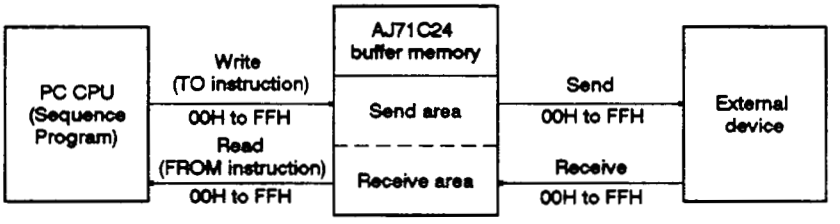
If these interfaces are used with the dedicated protocol in the bidirectional mode, it is not necessary to read this section.

9.1 Basics of the No-Protocol Mode

(1) What no-protocol mode means

In no-protocol communication:

- Data written to the no-protocol AJ71C24 send area (in buffer memory) using the TO instruction in a sequence program is output to an external device in the same code.
- Data received from an external device is read from the no-protocol AJ71C24 receive area (in buffer memory) using the FROM instruction in a sequence program.



POINT

In the no-protocol mode, data is not converted to ASCII code in the AJ71C24. If ASCII code is required, data must be processed into ASCII code in a PC CPU or external device.

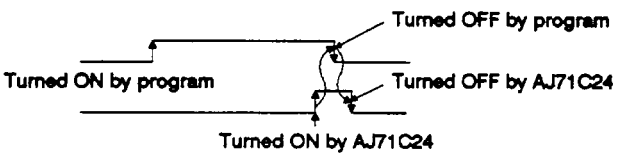
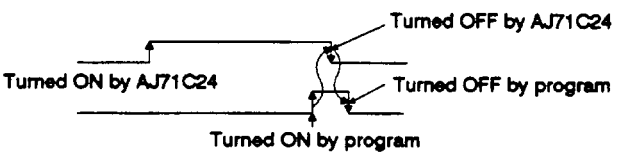
(2) Designating a word/byte unit for no-protocol mode communication

For data communications in the no-protocol mode, a unit of data to be transmitted may be selected between words and bytes. Default setting for data unit selection is "word", but selection is possible by writing "1" or "0" to address 103H in the buffer memory area.
(Section 7.4.3 gives details about the program to make this setting.)

9.2 Handshake I/O Signals

Signals known as I/O handshake signals are required for no-protocol communications.

These signals (a) output data received from the sequence program to an external device, or (b) detect signals from an external device to enable the sequence program to read them.

	Signal	Timing
PC CPU → External device	$Y_{(n+1)}0$ (Send request) X_n0 (Send completed)	
External device → PC CPU	X_n1 (Received data read request) $Y_{(n+1)}1$ (Receive data read completed)	

9.3 Programming Hints

9.3.1 To write data to the special use area in buffer memory

(1) Buffer memory is not backed up by a battery.

When the power is turned ON, the PC CPU is reset, or the mode is switched, all data in the buffer is set to default value.
Therefore, whenever the power is turned ON, the CPU is reset, or the mode is switched, any data which has been changed from a default value must be written to the buffer.

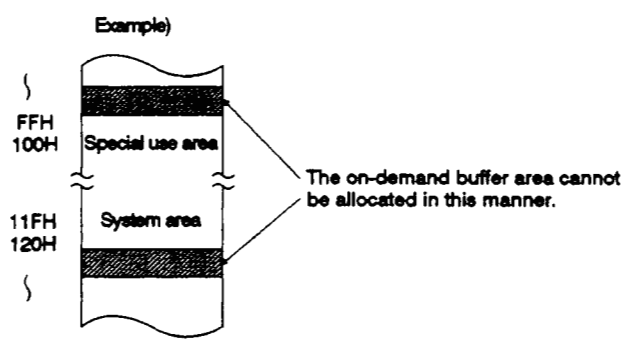
(2) Except for the mode switching area, data can only be written to the special applications area (100H to 11FH) using the TO instruction in a sequence program. If data is written to the buffer memory using the command in a computer program, the AJ71C24 will not operate correctly. Never try to write data using a computer program.

(3) If the following functions are used in combination with the dedicated protocol, make sure to allocate the user area in buffer memory so that the same area will not be used by different functions.

If the same area is allocated to different functions, the data in this area is rewritten and communications will not be correctly executed.

- No-protocol mode transmission or bidirectional mode transmission
- No-protocol mode receive or bidirectional mode receive
- Buffer memory read/write (CR/CW command) function
- On-demand function

The memory areas preceding and following the special use area cannot be allocated as a single area. The areas 0H to FFH and 120H to 7FFH must be recognized as independent areas.



(4) If the designation is made to process the send/receive data in the no-protocol mode or bidirectional mode in units of words or bytes, the on-demand data is processed in the same designated unit.

9.3.2 Precautions during data communications

(1) Communications with the computer in multidrop link. In the 1:n multidrop link, the data sent from the computer is received by each AJ71C24.

The message must contain the objective PC CPU where the data is sent and, at the same time, it is necessary to write the sequence program that ignores the received data addressed to other stations.

(Message example)

STX (02H)	Space (20H)	Station number 0 (30H)	Station number 2 (32H)	Data length (Binary data)	Data	CR (0DH)	LF (0AH)

(2) Conditions when the AJ71C24 transmission sequence is initialized

The transmission sequence is initialized in the following cases:

- When the power is turned ON, the PC CPU is reset by the reset switch, or the mode is switched
- The AJ71C24 CD signal is turned OFF during RS-232C full-duplex communications.

(If the CD signal is turned OFF during send or receive processing, data being processed for transmission or the data stored in the AJ71C24 receive data storing OS area is cleared.
In full-duplex communications, keep the CD signal ON.
The ON/OFF status of the CD signal is ignored if "CD terminal check disabled" is set at 10BH of the buffer memory address.)

(3) NULL code transmission from the AJ71C24

A framing error might occur at the AJ71C24 if nothing is sent from the computer to the AJ71C24 via the RS-422 interface. In this case, the AJ71C24 sends "00H" (NULL code) to the computer. This NULL code should be ignored by the computer.

(4) Combined use with dedicated protocols

When data communications is executed in the no-protocol mode, if the AJ71C24 mode setting switch (see Section 4.3.1) is placed in any position from 1 to 8, or any mode number from 1 to 8 is designated by the mode switching function, data communications with the other interface can be executed using the dedicated protocol.

Data communications cannot be executed by setting one interface to the bidirectional mode and the other to the no-protocol mode.

(5) Using a FROM/TO instruction to access the AJ71C24

A FROM/TO instruction to access the AJ71C24 from a PC CPU should only be used when absolutely necessary.

This is because when data is transmitted from the AJ71C24 to an external device at the same time a FROM/TO instruction from a PC CPU to the AJ71C24 is executed, the FROM/TO instruction has priority and is processed first.

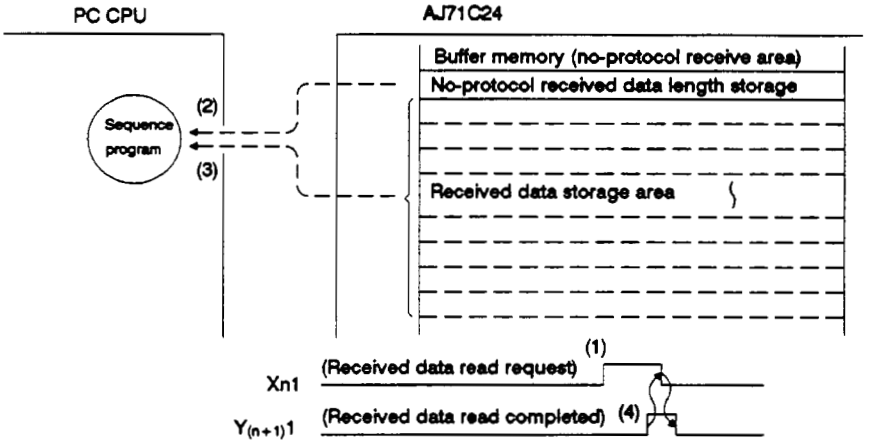
This delays the data send time from the AJ71C24 by how long it takes to process the FROM/TO instruction.

9.4 Basic Program to Read/Write Buffer Memory

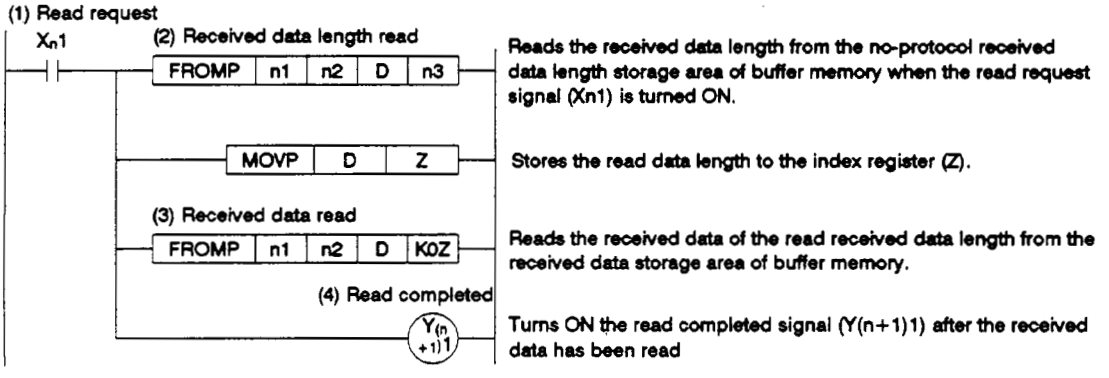
The following describes a basic sequence program to read and write data to and from the AJ71C24 buffer memory.

(1) Reading data from the receive area (FROM, FROMP, DFRO, DFROP)

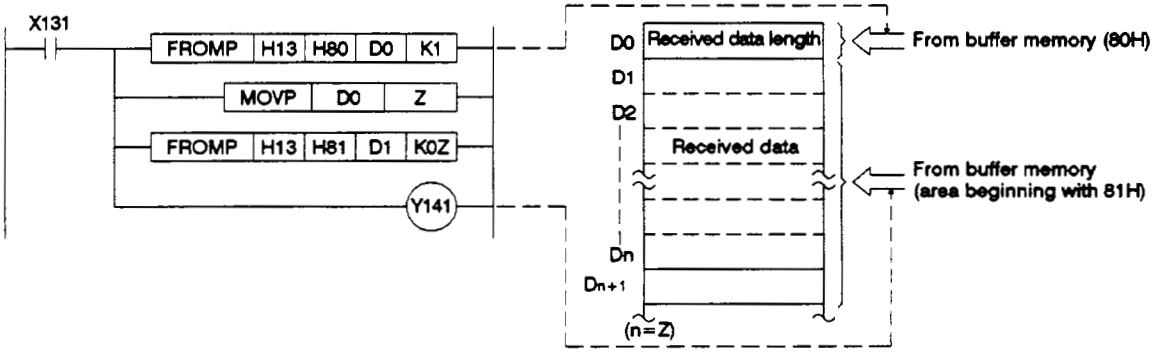
Data is read from the buffer memory no-protocol receive area (default: 80H to FFH).



Format

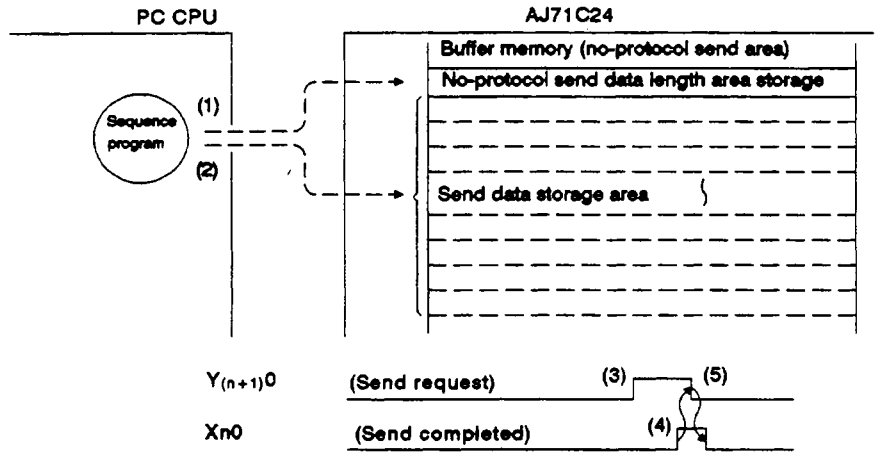

(1) Read request
Xn1
(2) Received data length read
FROMP n1 n2 D n3
Reads the received data length from the no-protocol received data length storage area of buffer memory when the read request signal (Xn1) is turned ON.
MOVP D Z
Stores the read data length to the index register (Z).
(3) Received data read
FROMP n1 n2 D K0Z
Reads the received data of the read received data length from the received data storage area of buffer memory.
(4) Read completed
Y(n+1)1
Turns ON the read completed signal (Y(n+1)1) after the received data has been read
* Data read by program 3) is processed as the received data.

Example: To read the data of (n+1) words from the area, beginning with buffer memory address 80H, to the area beginning with D0 when the AJ71C24 I/O numbers are allocated to 130 to 14F.

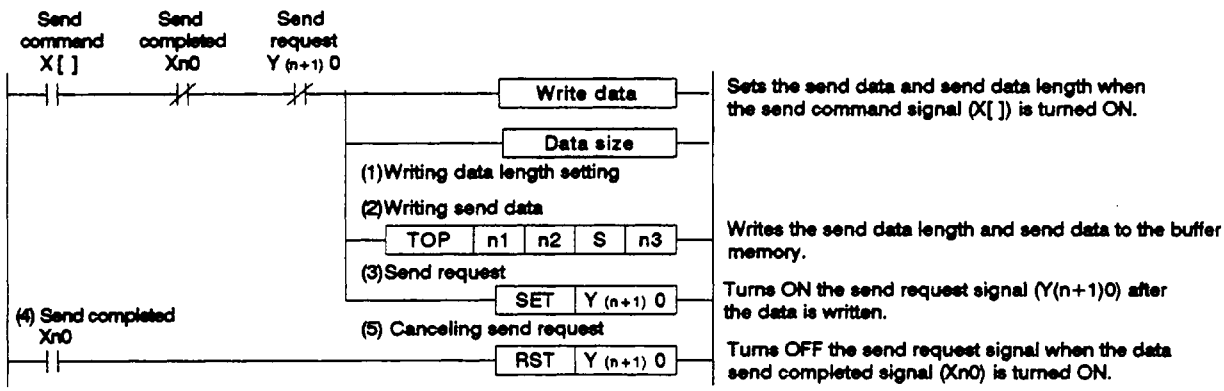


(2) Writing data to the send area (TO, TOP, DTO, DTOP)

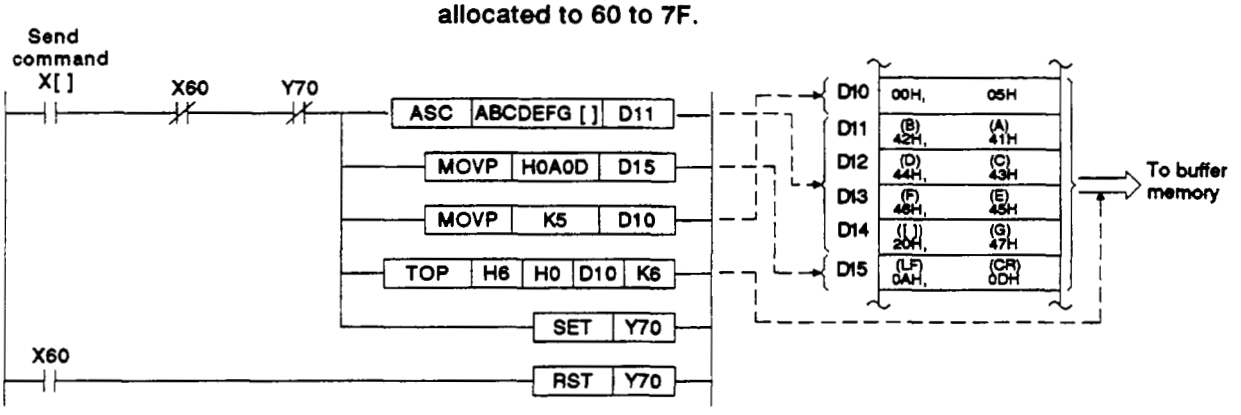
Data written to the no-protocol send area (default: 0H to 7FH).



Format


Send command X[ ]
Send completed Xn0
Send request Y(n+1) 0
Write data
Data size
(1)Writing data length setting
(2)Writing send data
TOP n1 n2 S n3
(3)Send request
SET Y(n+1) 0
(4) Send completed Xn0
(5) Canceling send request
RST Y(n+1) 0
Sets the send data and send data length when the send command signal (X[ ]) is turned ON.
Writes the send data length and send data to the buffer memory.
Turns ON the send request signal (Y(n+1)0) after the data is written.
Turns OFF the send request signal when the data send completed signal (Xn0) is turned ON.

(Example): To transmit 5-word data after writing "ABCDEFG [ ] CR.LF" to the *buffer memory* area from 1H when the AJ71C24 I/O numbers are allocated to 60 to 7F.



POINT

With an A2ACPU(S1) and A3ACPU, it is possible to execute communications with an external device using the dedicated instructions for the A2ACPU(S1) and A3ACPU.

For these dedicated instructions, see the AJ71C24(S3) computer link module control instructions in the A2A(S1)/A3A Programming Manual (Dedicated Instructions).

9.5 Receiving Data in the No-Protocol Mode (External Device → AJ71C24)

(1) Data receive area

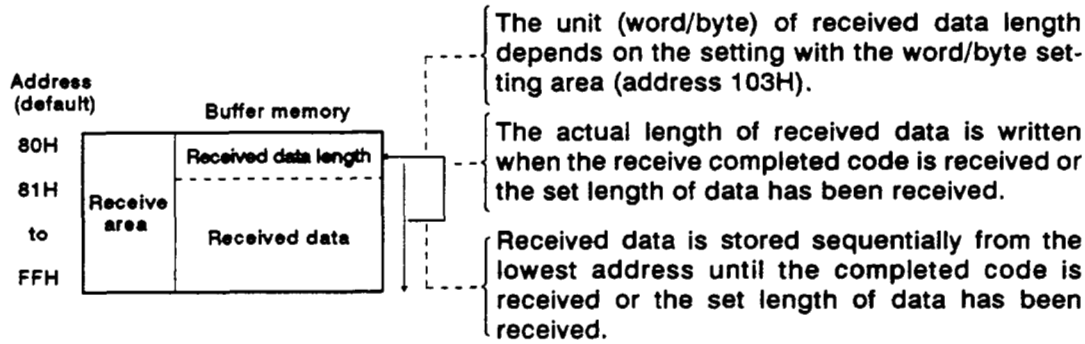
The AJ71C24 stores the received data length and received data in the data receive area.

With default setting, buffer memory area 80H to FFH is allocated as the receive area.

This area may be changed as needed. See Section 6.4.5 for the procedure to change the data receive area.

For example, if the data to be received is greater than the AJ71C24 receive area (127 words in default setting), data is received in more than one transmission.

It is advisable to set as "data receive area" is larger than "received data length".


Address (default)
Buffer memory
80H
81H
to
FFH
Receive area
Received data length
Received data
The unit (word/byte) of received data length depends on the setting with the word/byte setting area (address 103H).
The actual length of received data is written when the receive completed code is received or the set length of data has been received.
Received data is stored sequentially from the lowest address until the completed code is received or the set length of data has been received.

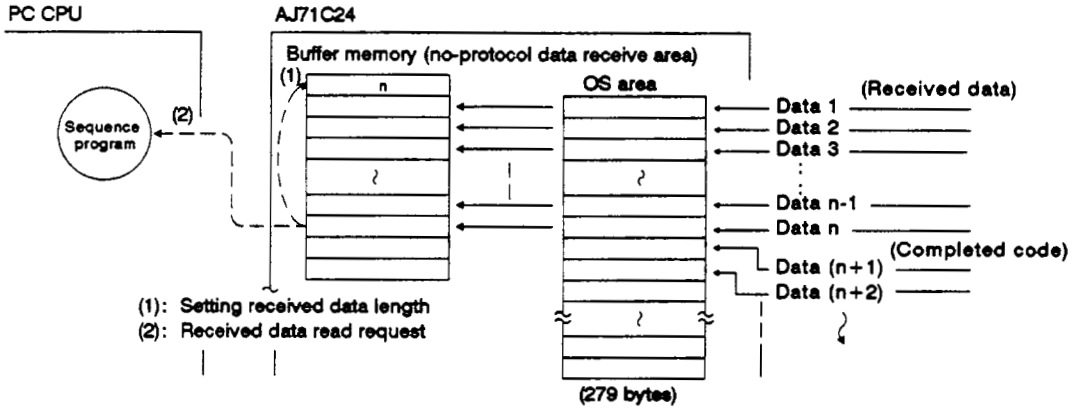
(2) Reading received data

There are two ways of making a request to read the received data:

- By receiving the receive completed code (data receive in variable length), and
- By receiving the set length of data (data receive in fixed length).

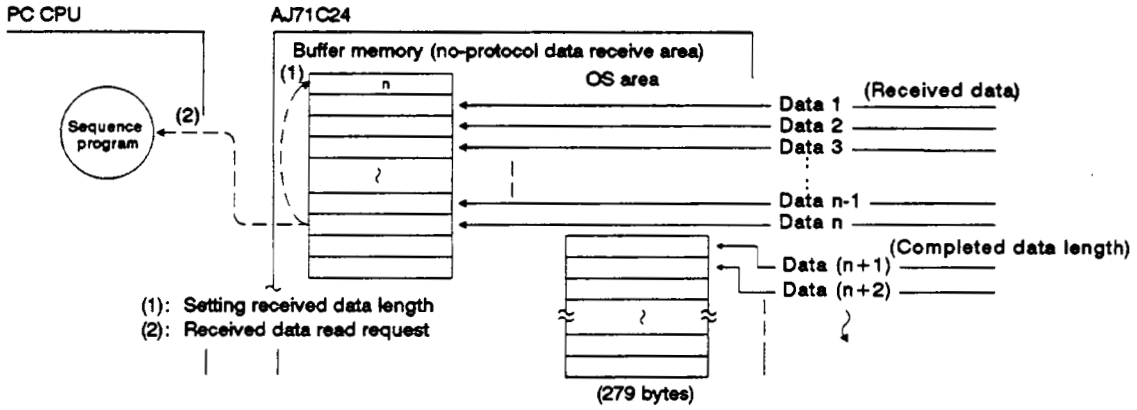
(a) By receiving the receive completed code (variable length)

The AJ71C24 makes a request to read the received data to the sequence program when it receives the receive completed code, predetermined by the user and set to the AJ71C24 buffer memory. The default receive completed code is CR, LF (0D0AH), but this may be changed to any value in the range of 0000H to 00FFH. (For the procedure to change the read completed code, see Section 7.4.1.)



(b) By receiving the set data length (fixed length)

The AJ71C24 makes a request to read the received data to the sequence program when it has received the set length of data from an external device.
Using this method, it is possible to receive fixed length data.
Default setting is 127 words, but this value may be changed as required. (For the procedure to change the data length setting, see Section 7.4.2.)



POINTS

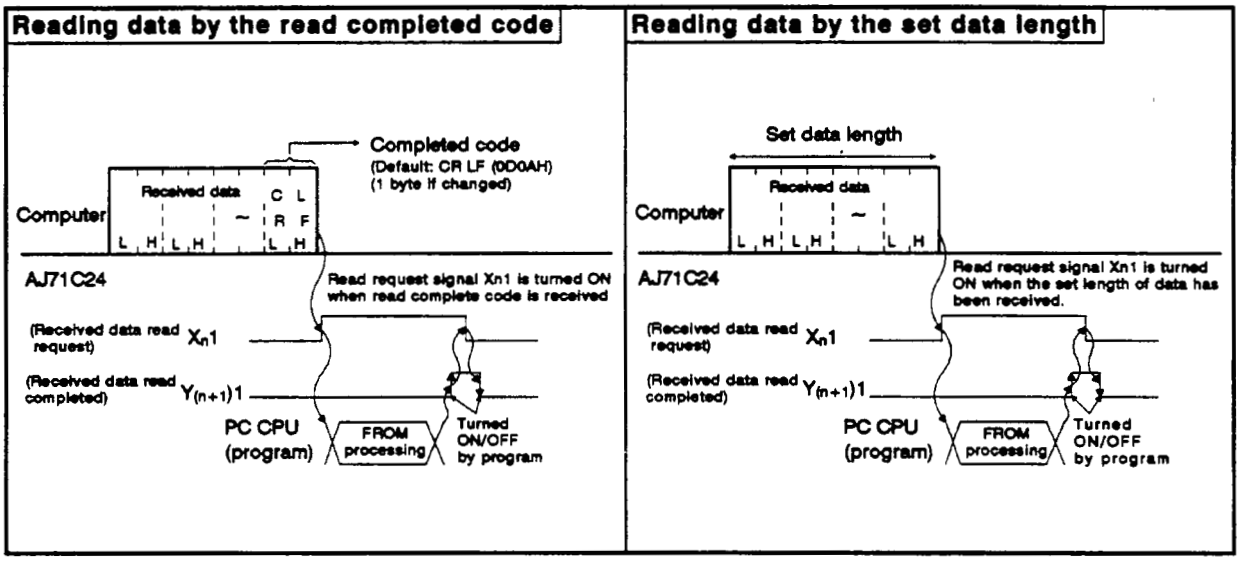
(1) When both the receive completed code and the receive completed data length are set to the special application area in buffer memory, both of them are effective.

In this case, the one which is met first triggers the read request signal (Xn1) to the sequence program. See Section 7.4.1 and 7.4.2.

(2) The data received after the reception of the receive completed code or the set length of data has been received is stored in the OS area (279 bytes) of the AJ71C24. The data stored in the OS area is transferred to the data receive area after the data previously stored in this area has been read by the sequence program.

In data communications through the RS-232C interface, the DTR signal is turned OFF when DTR/DSR control is executed. DC3 code is sent when DC1/DC3 transmission control is executed to request disconnection of data transmission from an external device because the OS area where receive data is stored is smaller than 10 bytes. See Sections 3.5.2 and 3.5.3.

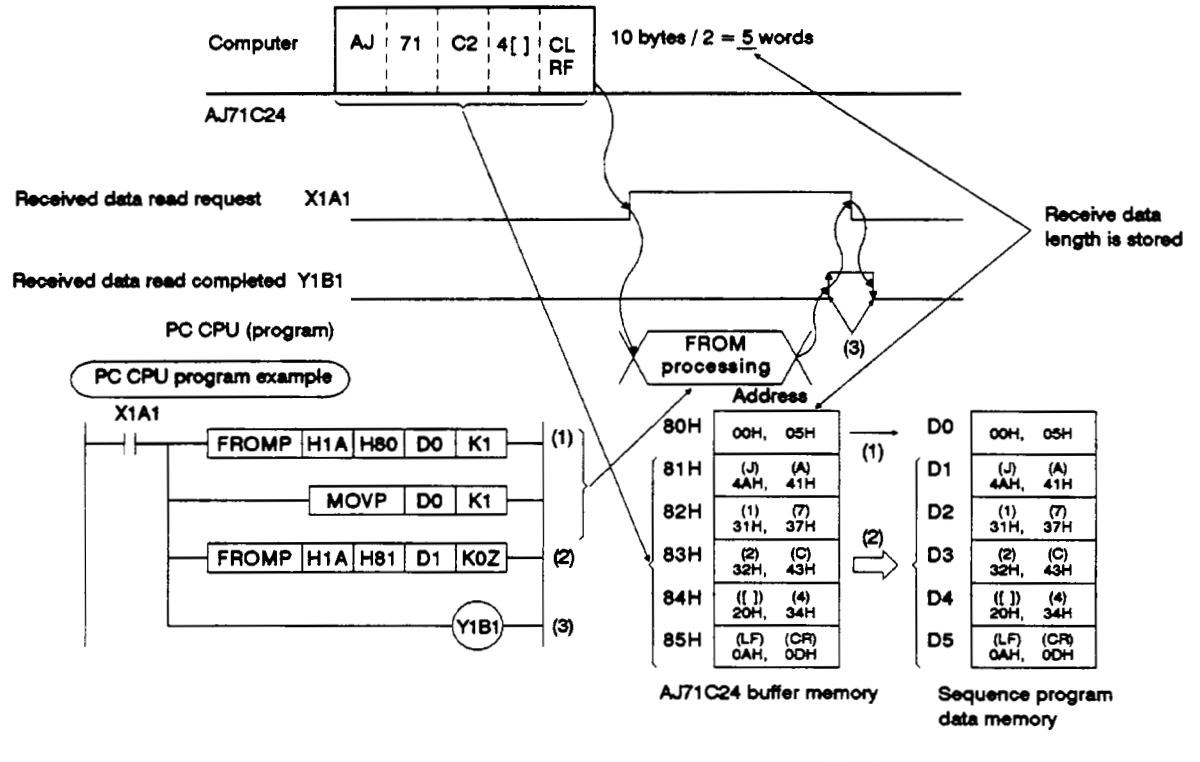
(3) Data receive procedure


Reading data by the read completed code
Completed code
(Default: CR LF (0D0AH)
(1 byte if changed)
Computer
Received data
C L
R F
L H L H L H
AJ71C24
Read request signal Xn1 is turned ON when read complete code is received
(Received data read request) Xn1
(Received data read completed) Y(n+1)1
PC CPU (program)
FROM processing
Turned ON/OFF by program
Reading data by the set data length
Set data length
Computer
Received data
L H L H L H
AJ71C24
Read request signal Xn1 is turned ON when the set length of data has been received.
(Received data read request) Xn1
(Received data read completed) Y(n+1)1
PC CPU (program)
FROM processing
Turned ON/OFF by program

(4) Data receive program examples

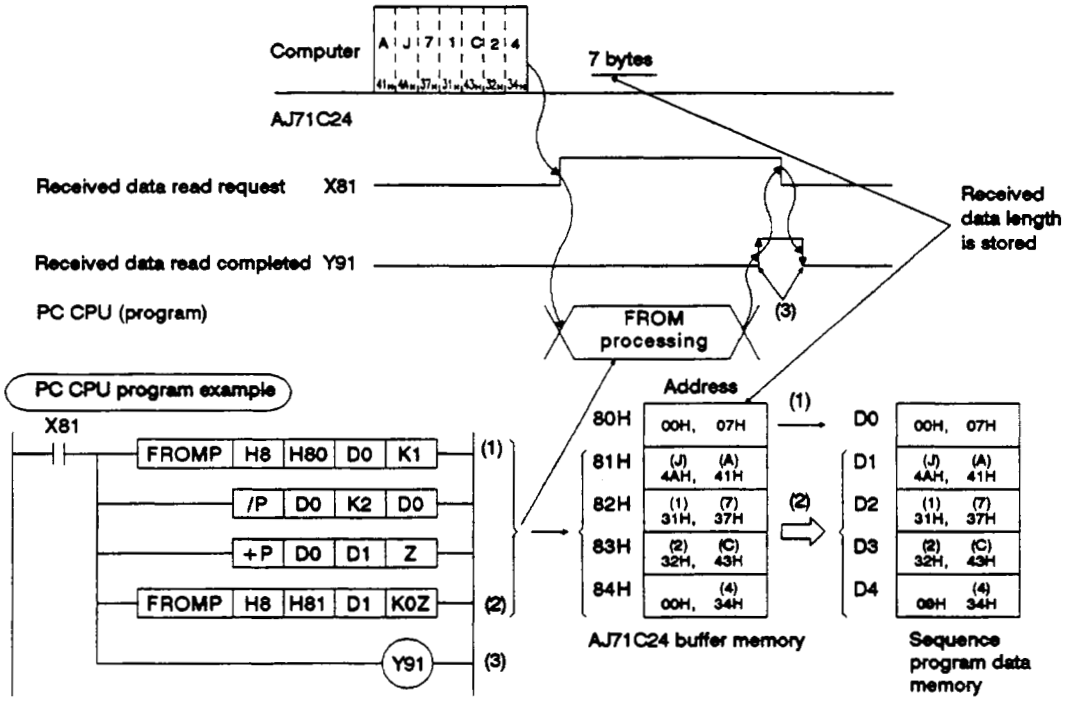
Example 1 : By receiving completed code, in word units (buffer memory allocation: default)

To store "AJ71C24[ ]" CR, LF, received from an external device, to D0 to D5 of PC CPU.
(AJ71C24 I/O addresses: 1A0 to 1BF)



Example 2: By receiving the set length of data, in byte units (receive area allocation default)

To receive "AJ71C24" from an external device and to store it to D0 to D4 of PC CPU with the following setting. (AJ71C24 I/O address: 80 to 9F)



POINT

- Even if transmission data units are set to byte units, the FROM instruction in a sequence program operates in word units. Therefore, the length of receive data must be converted to the number of buffer memory points (word units).

  In the above example, 7 bytes of data must be converted into 4 words (7 ÷ 2 = 3.5...).

- When an odd number of bytes of data is received, the higher 8 bits of the last address read by the FROM instruction are "00H".

REMARK

If the receive data length exceeds the no-protocol mode receive buffer memory size, the data is processed as described below.

(1) When the receive completed code is used:

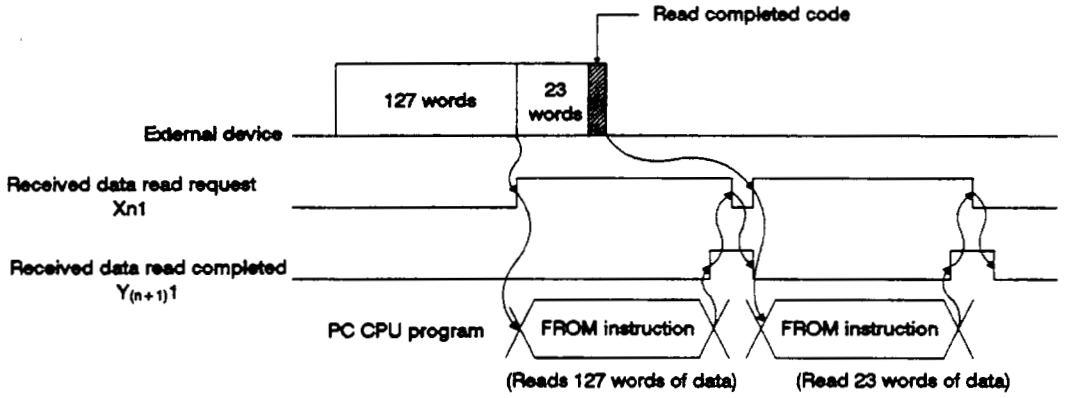
If the AJ71C24 receives data that exceeds the receive area size, it turns ON the received data read request signal Xn1 when data equivalent to the receive area size has been received.

Reading the remaining data is enabled at the time the sequence program turns the receive data read completed signal Y(n+1)1 ON.

These steps are repeated until the receive completed code is received.

Set the receive area size so that "receive-completion data length" is less than "no-protocol mode receive buffer memory size".

Example: To receive 150 words of data while receive area is set at 80H to FFH (default).

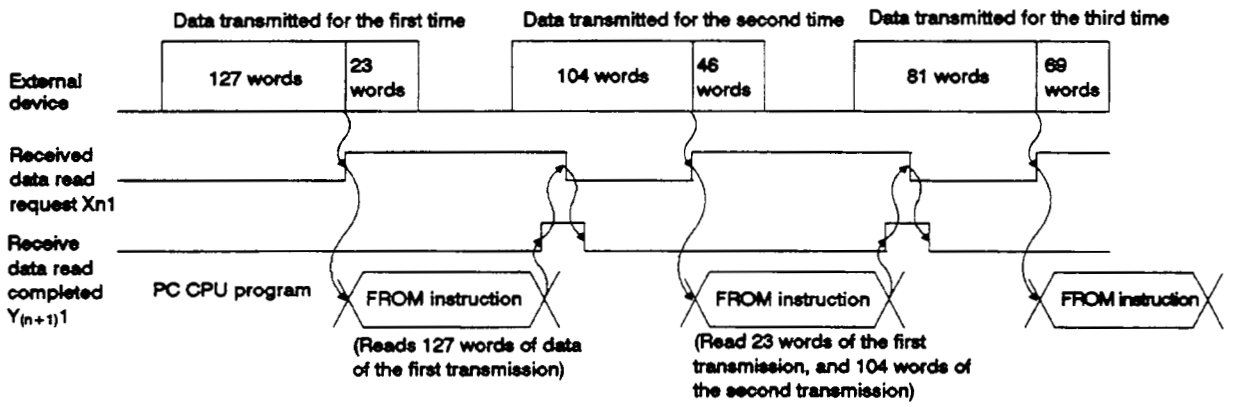


(2) When receive completion data length is used:

If the receive completion data length is set greater than the receive area size, the no-protocol receive buffer memory size (default: 127 words) which is set at buffer memory address 107H is taken as the receive completion data length.

Set the receive area size so that "receive completion data length" is less than "no-protocol mode receive buffer memory size".

Example: To receive 150 words of data while receive area is set at 80H to FFH (default setting).


Data transmitted for the first time
Data transmitted for the second time
Data transmitted for the third time
External device
127 words
23 words
104 words
46 words
81 words
69 words
Received data read request Xn1
Receive data read completed Y(n+1)1
PC CPU program
FROM instruction
FROM instruction
FROM instruction
(Reads 127 words of data of the first transmission)
(Read 23 words of the first transmission, and 104 words of the second transmission)

(5) Clearing the receive buffer memory

If and error occurs due to failure of an external device, for example, while receiving data from an external device in the no-protocol mode, the data received up to the error may be incorrect or interrupted. To received up to the error may be incorrect or interrupted. To recover after an error has occurred it is possible to cleaa all received data and initialized the AJ71C24 buffer memory.

(a) Error detection

The following methods are used to detect errors while data is being received.

1) Reading the error LED display area

To detect errors the PC CPU can read the LED ON/OFF statuses, stored at buffer memory address 101H as transmission error data.

2) PC input signals

Signals such as READY signals from external devices are connected to the PC CPU as input signals. The PC CPU can detect errors from the ON/OFF status of these signals.

(b) Clearing received data

1) Range of data cleared

All data already received by the AJ71C24 is cleared and the no-prptocol mode receive buffer memory area is initialized (See Section 3.5.2 and 3.5.3 for details).

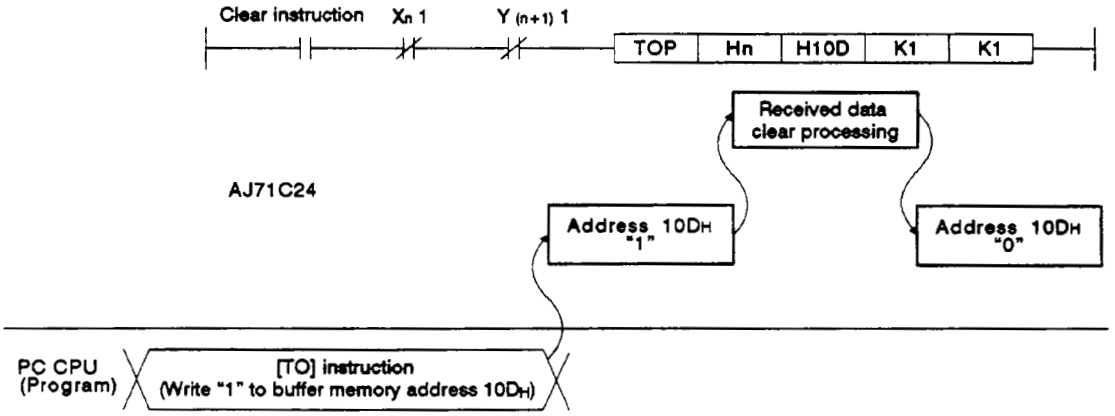
2) How to clear received data

Received data is cleared by writing "1" to buffer memory address 10DH using the [TO] instruction.

After clearing received data, the AJ71C24 clears the "1" that was written to buffer memory address 10DH.

The received data may be cleared while the receive data read request signal (Xn1) and received data read completed signal (Y(n+1)1) are OFF.

Use Xn1 and Y(n+1)1 as an interlock for TO instruction.



9.6 Sending Data in the No-Protocol Mode (AJ71C24 → External Device)

In this section, "sending" means outputting data which is in the no-protocol mode AJ71C24 send area to an external device receive area. This is in response to turning the PC CPU send request signal (Y(n+1)0) ON.

(1) Send area and writing send data

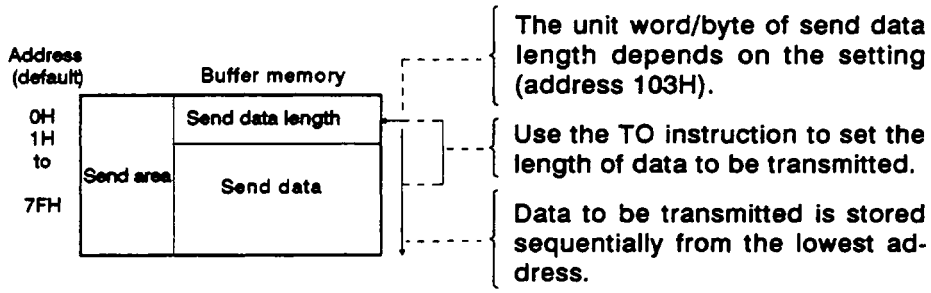
The send data length and send data are written to the send area.

(a) The length of send data to be written (or having been written) to the send data storage area is written to the no-protocol send data length storage area in either words or bytes.

(b) The data to be transmitted is written to the send data storage area.

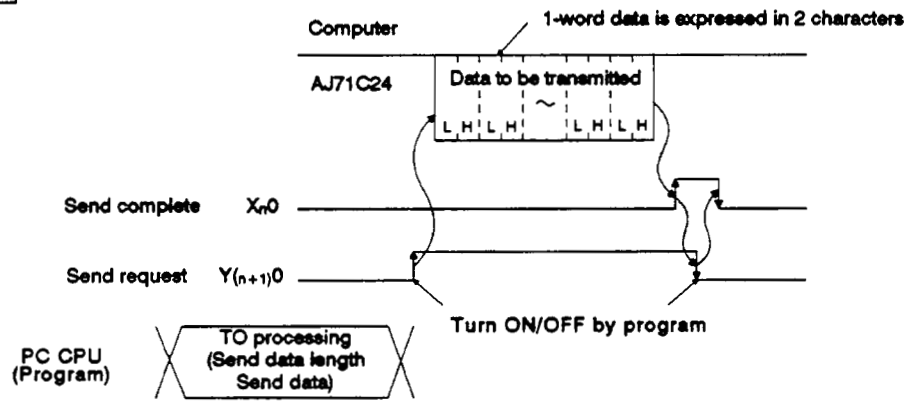
When the send request signal (Y(n+1)0) is turned ON after (a) and (b) have been executed, the AJ71C24 transmits the set length of set data from the send data storage area in the order of address number.

By default, buffer memory area 0H to 7FH is allocated to the AJ71C24 send area.
It is however possible to change the send area allocation. (See Section 7.4.4.)


Address (default)
Buffer memory
0H
1H
to
7FH
Send area
Send data length
Send data
The unit word/byte of send data length depends on the setting (address 103H).
Use the TO instruction to set the length of data to be transmitted.
Data to be transmitted is stored sequentially from the lowest address.

(2) Data sending procedure

Procedure


Computer
1-word data is expressed in 2 characters
AJ71C24
Data to be transmitted
L H L H ~ L H L H
Send complete XnO
Send request Y(n+1)0
Turn ON/OFF by program
PC CPU (Program)
TO processing (Send data length Send data)

POINTS

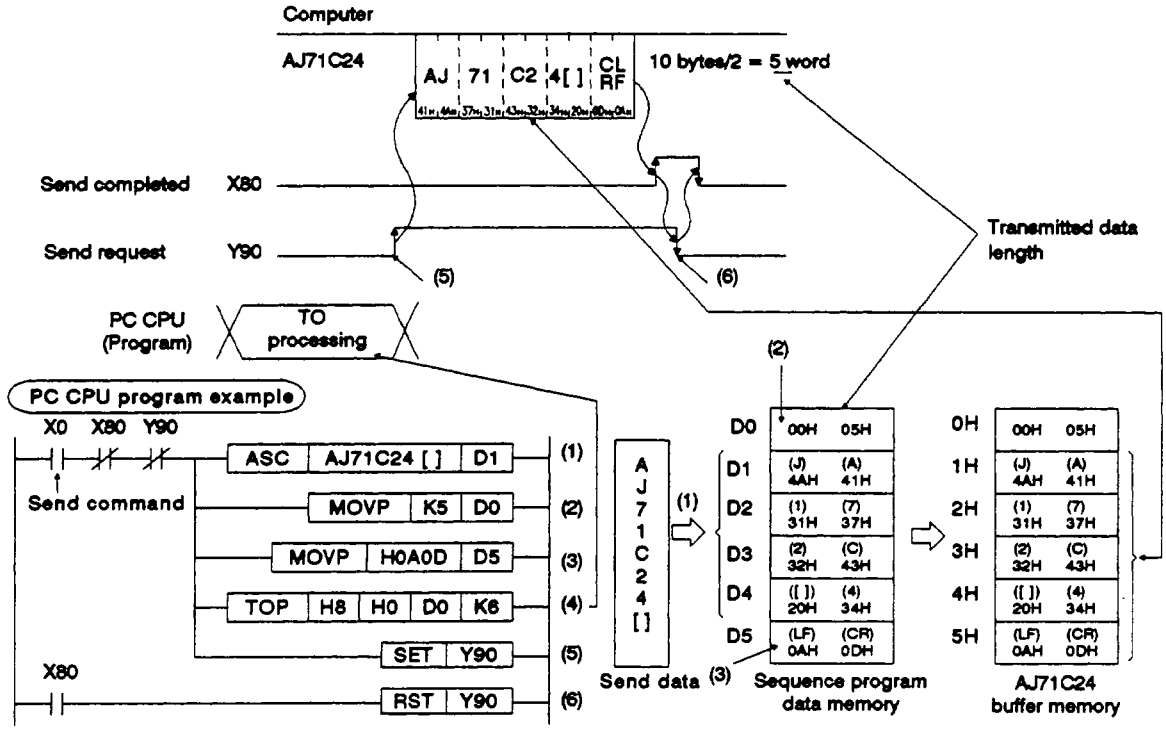
(1) An error occurs if the send data length is greater than the send area, or equal to "0". In this case, "1" is written as transmission error information to the most significant bit (bit 15) of address 101H (error LED display area) in the special application memory area. (See Section 7.3.1.)

(2) The send data length written to the head address of the send area is not transmitted.

(3) Data transmission program examples

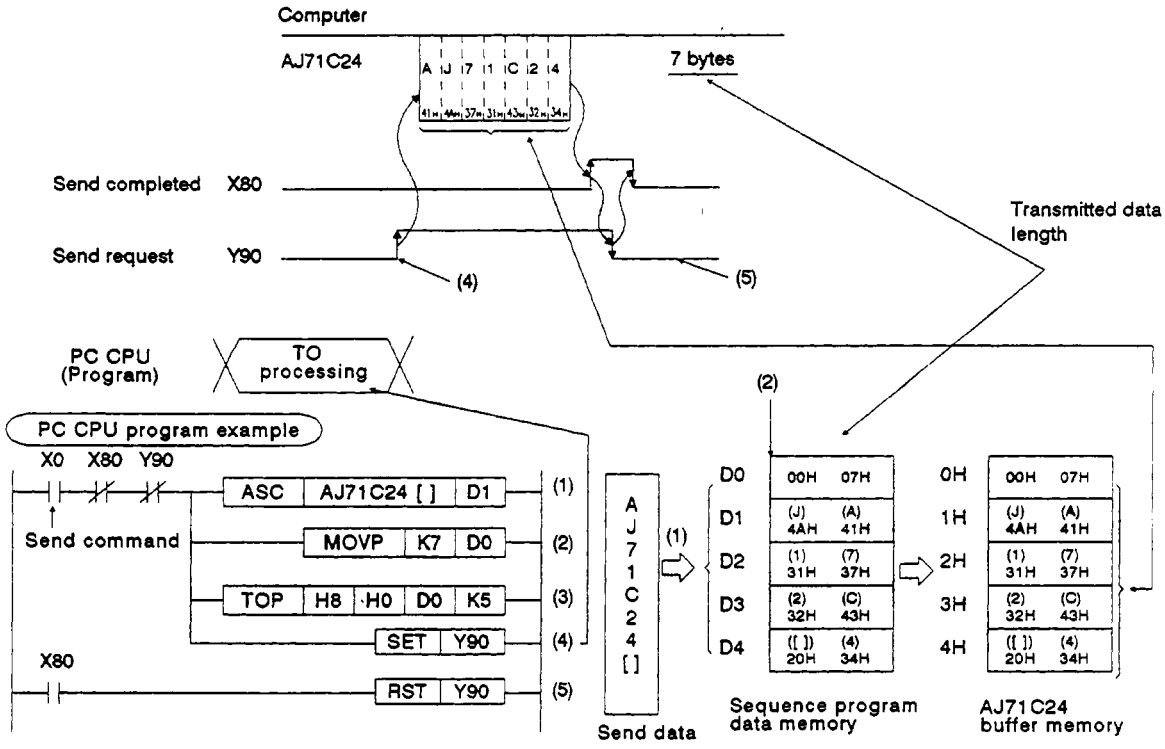
Example 1: Transmitting data in word units (buffer memory allocation: default)

To write "AJ71C24[ ]"CR, LF by sequence program and transmit it to an external device (AJ71C24 I/O addresses: 80 to 9F)



Example 2: Transmitting data in byte units (buffer memory allocation: default)

To write "AJ71C24[ ]"CR, LF by sequence program and transmit it to an external device ((AJ71C24 I/O addresses: 80 to 9F)



POINT

Even if transmission data units are set byte units, the TO instruction in a sequence program operates in word units. Therefore, the length of send data differs from the data length set with the TO instruction.

10. COMMUNICATIONS IN THE BIDIRECTIONAL MODE

Bidirectional communications with a computer is possible only when a computer and an AJ71C24 are linked in a 1 : 1 ratio.

Always read this section when the RS-422 and RS-232C interfaces are used with a dedicated protocol and in the bidirectional mode with the mode setting switch of the AJ71C24 being set to any position from "1" to "8" or with the mode switching function being used to set the mode number to any of "1" to "8".

It is not necessary to read this section when the interfaces are used with a dedicated protocol and in the no-protocol mode.

POINT

Buffer memory used in the bidirectional mode

In sections other than this, buffer memory used in the bidirectional mode is described as the buffer memory used for the no-protocol mode. Because the application purposes are the same, simply think of the "no-protocol mode" as the "bidirectional mode".

Examples:

- No-protocol mode send area
  → Bidirectional mode send area
- No-protocol send buffer memory head address setting area
  → Bidirectional send buffer memory head address setting area

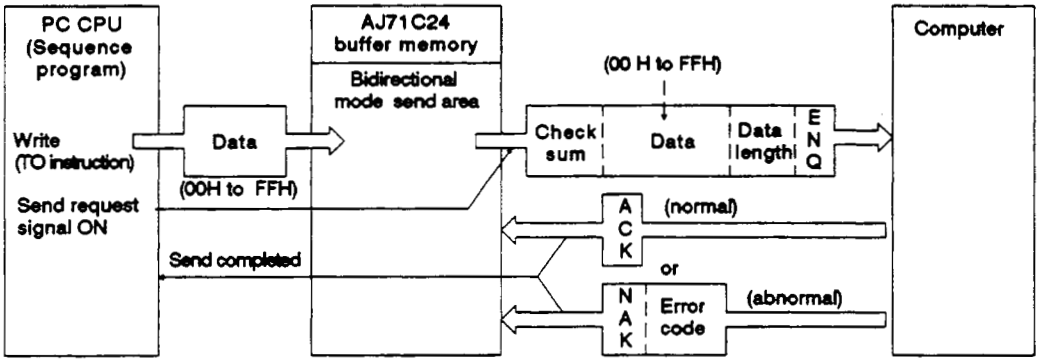
10.1 Bidirectional Mode Basics

(1) What bidirectional mode means

In bidirectional communications:

The bidirectional receive/send area in an AJ71C24 buffer memory is used for data commuications with a computer.

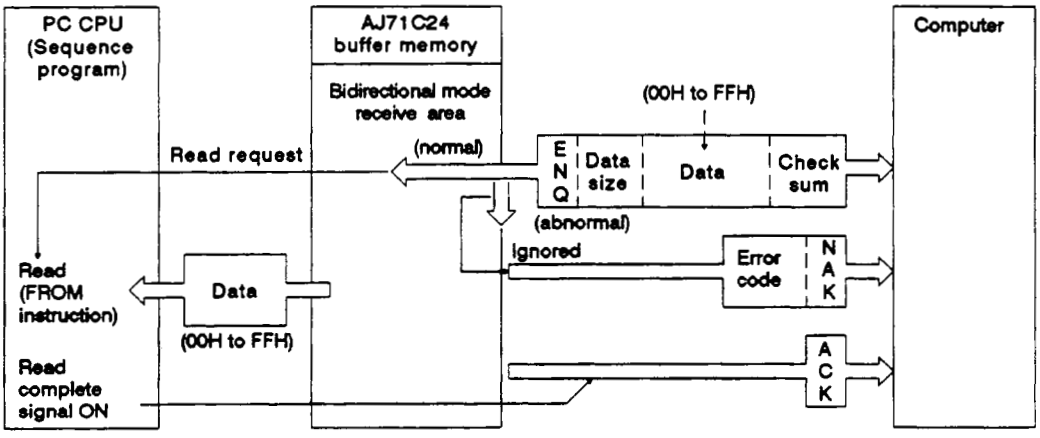
The data written to an AJ71C24 buffer memory by the TO instruction in a sequence program is transmitted to a computer in the same code with the control code (ENQ=05H) prefixed to the data to be transmitted.



An AJ71C24 receives a response from a computer.

The data received from a computer is stored in an AJ71C24 received area and read by the FROM instruction in the sequence program (the data received is transferred in the code as received).

The response data is transmitted to a computer in response to the read completed signal.



POINT

In the bidirectional mode, data is not converted to ASCII code in the AJ71C24. When ASCII code is required, the data must be processed into ASCII code in a PC CPU or computer.

(2) Designating word/byte units for bidirectional mode communications

For data communications in the bidirectional mode, units of data to be transmitted may be selected between words and bytes. Default setting for data unit selection is "word", but selection is possible by writing "1" or "0" to address 103H in the buffer memory area.

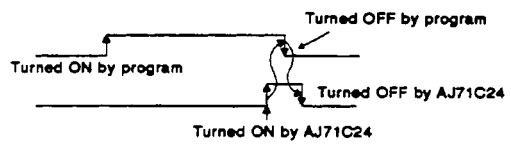
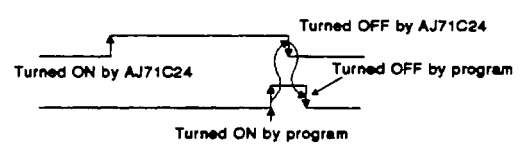
(Section 7.4.3 gives details of the program to make this setting.)

10.2 Handshake Signals and Buffer Memory

(1) Handshake signals in the bidirectional mode

Signals known as I/O handshake signals are required for communications in the bidirectional mode.

These signals output data received from the sequence program to a computer or detect signals from an external device to enable the sequence program to read them.

	Signal		Timing
PC CPU ↓ Computer	Y (n+1) 0	(Send request)	
	X n 0	(Send completed)	
Computer ↓ PC CPU	X n 1	(Received data read request)	
	Y (n+1) 1	(Receive data read complete)	

The number "n" appended to X and Y is determined according to the position where the AJ71C24 is loaded and the number of I/O modules loaded prior to this module. If this module (AJ71C24) is loaded at slot 0 in a base module, Xn0 is expressed as "X0".

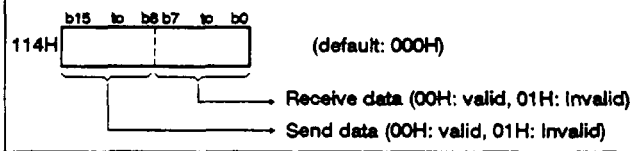
(2) Buffer memory used in the bidirectional mode

(a) Special applications area (100H to 1FFH)

Address	Name	Description
103H	Word/byte designation area for bidirectional mode	• The unit (word/byte) of data length of a message transmittted between a computer and a PC CPU is designated with a TO instruction in a sequence program. This sets the unit of data to be stored in the send data length storage area (default address 0H) and the received data length storage area (default address 80H). 0: Word (default) 1: Byte
104H	Bidirectional mode send buffer memory area head address designation area	• The head address of the area used for bidirectional mode send buffer memory area (send data length storage area and send data strage area) is designated with a TO instruction in a sequence program. • The area of the designated address is set as the send data length storage area. (0 to FEH or 20H to 7FEH : Bidirectional send buffer memory head address. (default : 0H)
105H	Bidirectional mode send buffer memory length designation area	• The length of the area used for bidirectional mode send is designated with a TO instruction in a sequence program. (default: 80H). When 0H to FFH area is used, 2H to 100H: Bidirectional send buffer memory When 120H to 7FFH area is used, 2H to 6E0H: Bidirectional send buffer memory length
106H	Bidirectional mode receive buffer memory area head address designation area	• The head address of the area used for bidirectional mode receive buffer area (receive data length storage area and receive data storage area) is designated with a TO instruction in a sequence program. • The area of the designated address is set as the receive data length storage area. 0H to FEH 20H to 7FEH: Bidirectional mode receive buffer memory head address. (default: 80H)
107H	Bidirectional mode receive buffer memory length designation area	• The length of the area used for bidirectional mode data receive is designated with a TO instruction in a sequence program (default: 80H). When 0H to FFH area is used, 2H to 100H: Bidirectional receive buffer memory length When 120H to 7FFH area is used, 2H to 6E0H: Bidirectional receive buffer memory length

(continued on page 10-6)

(continued)

Address	Name	Description
112H	Bidirectional mode designation area	• Whether the interface communications mode is no-protocol or bidirectional is designated with a TO instruction in a sequence program. 0: No-protocol mode (default) 1: Bidirectional mode
113H	Time-out check time designation area	• The time-out check time (until the reception of a response after transmission of data to the computer) is designated with a TO instruction in a sequence program. 0H : Time-out is not checked (default) 1H to FFFFH : Time-out check time (100 msec units) The most significant bit in the area is not regarded as the sign bit. The set value is regarded to designate value in the range of 1 through 65535.
114H	Data valid/invalid designation area at simultaneous transmission	• How the receive and send data at an AJ71C24 is processed if data transmission at a computer and an AJ71C24 occurs simultaneously is designated with a TO instruction on a sequence program. (Section 10.6 covers silmultaneous transmission) 
115H	Bidirectional mode check sum enable/disable designation area	• Whether or not check sum is appended for bidirectional mode communications is designated with a TO instruction in a sequence program. (This designation is not related to the setting of DIP switch SW21.) 0: Check sum enabled (default) 1: Check sum disabled
116H	Error storage area for data send	• If an error occurs during data communications, the error code is transmitted by an AJ71C24. (The area designated in 117H retains the error code of the last data receive error.) 0H : Normal termination (no error) 0001H to 0083H : Abnormal termination (error) Section 11.2 gives error code details.
117H	Error storage area for data received	

POINT

The area described above is the special applications area for bidirectional mode communications.

For other special applications areas used for data communications, see Section 3.5, section 5, and section 7.

(b) User areas (0H to FFH and 120H to 7FFH)

Address	Name	Description
0H to FFH and 120H to 7FFH	Send data length storage area	• The length (words or bytes) of data written to the send data storage area, to be transmitted from the AJ71C24 to the computer, is designated with a TO instruction in a sequence program • The set value is used as it is to designate data length in a message to be sent to the computer. • The unit of data length is determined by the value set at address 103H. • Set the send data length within the send data storage area length, described below.
	Send data length storage area	• The data to be transmitted to the computer is designated with a TO instruction in a sequence program. • The buffer memory length and length of the send data and send data length storage areas are determined by the values set at 104H to 105H. (Default: Send data length storage area address : 0H Send data storage area address : 1H to 7FH)
	Received data length storage area	• The data length in the message received from the computer is written by an AJ71C24 as it is as the received data length. Data length expresses the number of words/bytes at the data section in the message. • The unit of data length is determined by the value set at address 103H. • Transmit the data from the computer within the receive data storage area length described below.
	Received data length storage area	• The data in the data section in the message received from a computer is transmitted by the AJ71C24 as it is received. • The buffer memory length and length of the received data and received data length storage areas are determined by the values set at 106H to 107H. (Default: Received data length stora area address : 80H Received data storage area address : 81H to FFH)

10.3 Programming Hints

10.3.1 System configuration and communications mode for bidirectional mode communications

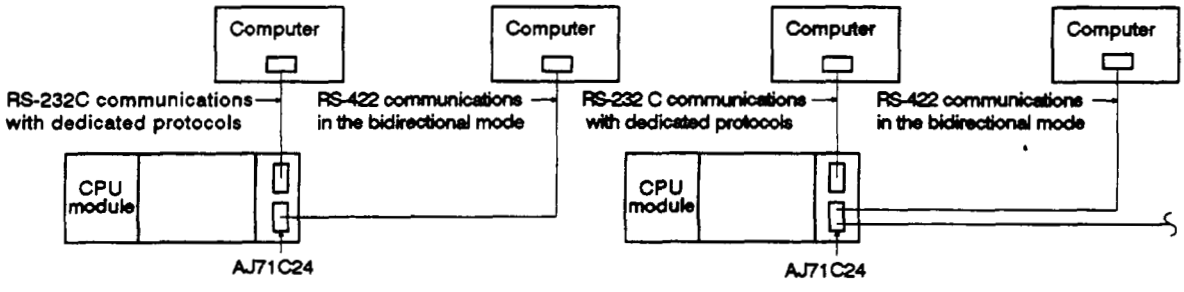
(1) System configuration and the AJ71C24 mode setting

Data communications in the bidirectional mode is possible only in the system where a computer and the AJ71C24 are linked in a 1 : 1 ratio. The mode setting switch in the AJ71C24 should be set in any position of "1" to "8", or the mode switching function can be used to set the mode number from "1" to "8" (see Sections 3.4 and 7.6.2).

(2) Usable with dedicated protocols

When data communications is executed in the bidirectional mode, data communications using the dedicated protocol is possible with the other interface.

Data communications using the bidirectional mode and the no-protocol mode at the same time is not possible.



10.3.2 To write data to a special applications area in buffer memory

(1) Buffer memory is not battery backed up by a battery

When the power is turned ON, the PC CPU is reset, or the mode is switched, all data in the buffer memory is set to the default values.

Therefore, any data changed from the default values must be written whenever the power is turned ON, the PC CPU is reset, or the mode is switched.

(2) Except for mode switching areas, only a TO instruction can be used to write data to the special applications area (100H to 11FH).

(3) If data is written using the command in a computer program, the AJ71C24 will not to operate correctly. Never try to write data using a computer program.

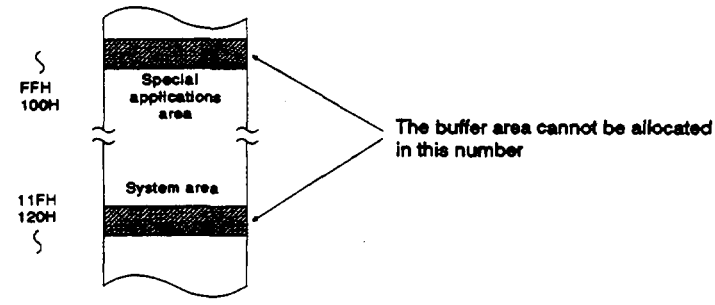
If the following functions are used in combination with the dedicated protocol, allocate the user area in buffer memory so that the same area will not be used by different functions.

If the same area is allocated to different functions, the data in this area is rewritten and communications will not be correctly executed.

- Bidirectional mode send
- Bidirectional mode receive
- Buffer memory read/write (CR/CW command) function
- On-demand function

The memory areas preceding and following the special applications area cannot be allocated as a single area. The areas of 0H to FFH and 120H to 7FFH must be recognized as independent areas.

Example:



(4) If designation is made to process the send/receive data in the bidirectional mode in units of words or bytes, the on-demand data with the dedicated protocol is processed in the same designated unit.

(5) Do not write "1" (request to clear) to the bidirectional received data clear request area (address 10DH).

If "1" is written, all received data may be cleared, and data communications might not be correctly executed.

10.3.3 Precautions during data communications

(1) The conditions under which the AJ71C24 transmission sequence is initialized are as follows:

- The power supply is turned ON, the PC CPU is reset with the reset switch, or the mode is switched.
- Data communications has completed normally.
- The response message (ACK or NAK) is transmitted.
- During full-duplex communications through the RS-232C interface, the CD signal is turned OFF.

(The ON/OFF status of the CD signal is ignored if the CD terminal check function is disabled.)

(2) Send request signal made by the computer

To transmit data from an AJ71C24 send area to a computer receive area, follow the steps described in Section 10.9.

Once the send request signal (Y(n+1)0) is turned ON, do not turn it OFF until the send completed signal (Xn0) is turned ON.

When the send request signal is turned OFF by turning ON the send completed signal, read the error code storage area (116H) for data transmission to check the send result.

(3) Data send from the computer send area or AJ71C24 send area

To transmit data from a computer or AJ71C24 in the bidirectional mode, start data communications in sequence only after the receive/send of the response for the previous data send/receive has been completed.

(4) Data length

The data length in a message must be smaller than the send or receive data storage area that is set at the special applications area.

(a) Data transmitted from an AJ71C24 send area to a computer-receive area

Data length must be smaller than the send data storage area length [(set value at buffer memory address 105H) - 1 (words)].

(b) Data transmitted from a computer send area to AJ71C24 receive area

Data length must be smaller than the received data storage area length [(set value at buffer memory address 107H) - 1 (words)].

(5) NAK code

(a) Transmitting NAK from an AJ71C24 to a computer

The NAK response is given from an AJ71C24 to a computer if an error is detected.
Therefore, the NAK response might be given while the computer is transmitting data if communications is made in the full-duplex mode.

(An AJ71C24 ignores the designated length of received data if it detects an error while receiving data. If the data length is incorrect, the data received is ignored until the ENQ code is received.)

(b) Transmitting NAK from a computer to an AJ71C24

To transmit the NAK from a computer to an AJ71C24, transmit a 2-byte error code following the NAK code.

If the NAK code is received as the response, execute error processing according to the error code received directly after the NAK code.
The error codes related to the bidirectional mode communications are described in Section 11.2.

(6) Time-out check by a computer

If a time-out check is made for data transmitted from a computer send area to an AJ71C24 receive area in the bidirectional mode, the time-out check time to be set must be longer than the value shown below.
(Maximum scan time of the PC CPU x 2) + 100 msec

(7) NULL code send from an AJ71C24

A framing error might occur at the AJ71C24 if nothing is transmitted from a computer to an AJ71C24 via the RS-422 interface. In this case, the AJ71C24 sends "00H" (NULL code) to the computer receive area. These NULL codes should be ignored by the computer.
The computer should also ignore all data transmitted from the AJ71C24 prior to an ENQ, ACK, or NAK code.

(8) Using a FROM/TO instruction to access the AJ71C24

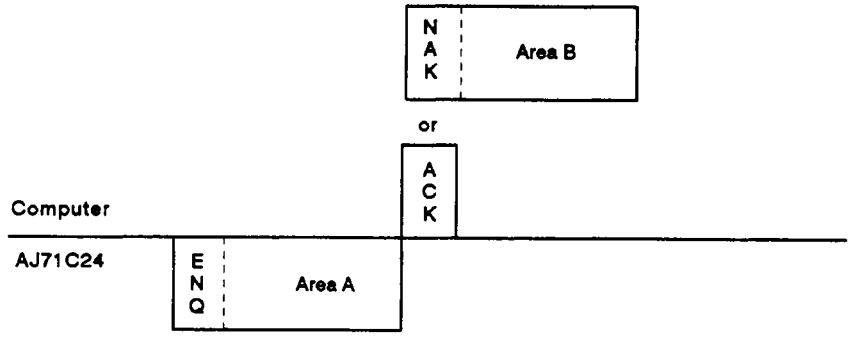
Using a FROM/TO instruction to access the AJ71C24 should not be done unless absolutely necessary. This is because when data is sent from the AJ71C24 to an external device at the same time as a FROM/TO instruction from a PC CPU is executed to the AJ71C24, the FROM/TO instruction has priority and is executed first. Therefore, the data send time from the AJ71C24 to the external device is delayed by the processing time of the FROM/TO instruction.

(9) Data bit setting

If a checksum is communicated during data communications with a computer, set the data bit (set with the SW12 switch) to eight bits. Section 4.3.2 gives details about switch SW12.

10.4 Bidirectional Control Procedure Basics

(1) Transmitting data from an AJ71C24 to a computer

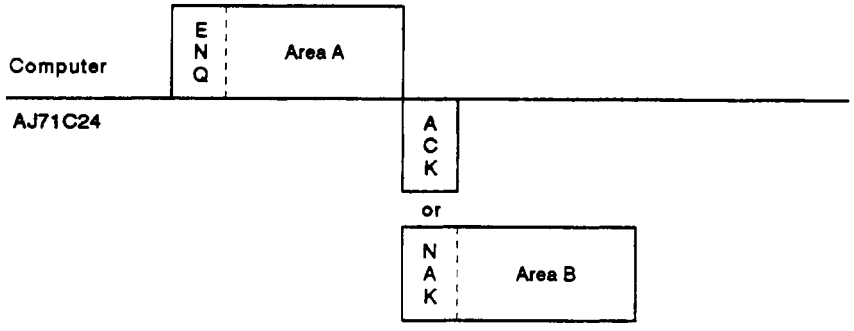


(a) Area A: Data send from an AJ71C24 to a computer

(b) Area B: Data send from a computer to an AJ71C24

(c) Write a program so that data is transmitted from left to right.
(Example: For area A, data is transmitted from ENQ to right)

(2) Transmitting data from a computer to an AJ71C24



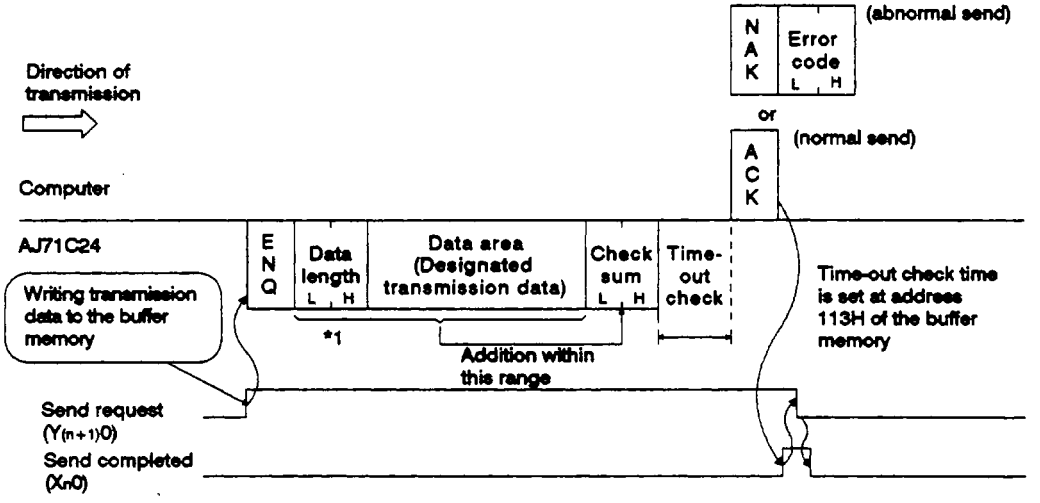
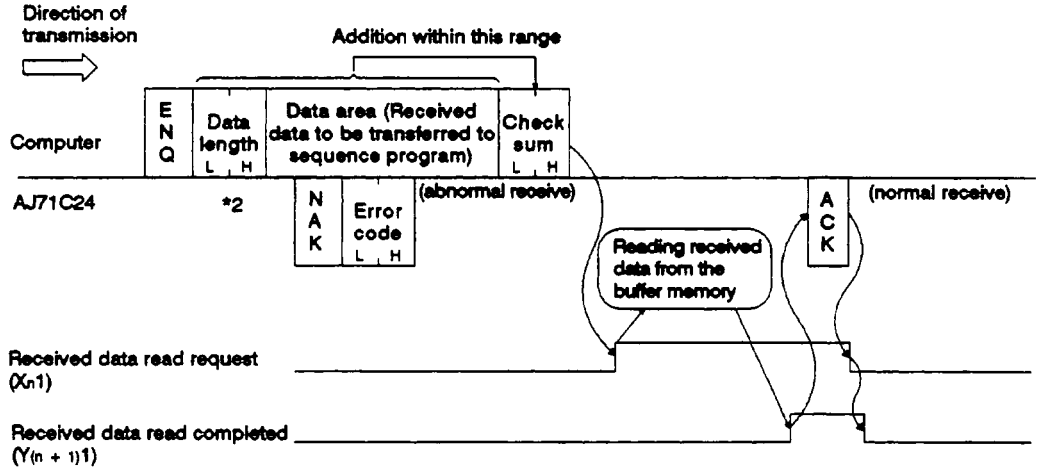
(a) Area A: Data send from a computer to an AJ71C24

(b) Area B: Data send from an AJ71C24 to a computer

(c) Write a program so that the data is transmitted from left to right.
(Example: For area A, data is transmitted from ENQ to right)

10.5 Bidirectional Communications Basics

10.5.1 Control protocols

<table>
<tr><th>Contents</th><th>Protocol</th></tr>
<tr><td>Transmission from a PC CPU to a computer</td><td> 
</td></tr>
<tr><td>An AJ71C24 receives data from a computer</td><td> 
</td></tr>
<tr><td>Remark</td><td>(1) Check sum exists only when "0" is set to address 115H of buffer memory.
(2) Check sum is calculated within the area indicated by *1.
(3) The AJ71C24 returns an NAK immediately if it detects an error as in *2 while communications is made in the full-duplex mode. In half-duplex mode communication, it returns an NAK only after the data has been received.
The AJ71C24 ignores receive data if it detects an error (Section 10.3.3 (5)). Therefore, it does not give a received data read request to the PC CPU.</td></tr>
</table>

10.5.2 Message format

(1) Control code

Signal Name	Code (hexadecimal)	Meaning	Application
ENQ	05H	Enquiry	The code used to begin data send.
ACK	06H	Acknowledge	The code returned to the mating station when data has been received correctly.
NAK	15H	Nagative Acknowledge	The code returned to the sending stations when data has not been receiving correctly. (immediately followed by an error code)

(a) Data send from an AJ71C24 to a computer

The AJ71C24 appends the control code to be transmitted.

(b) Data send from a computer to an AJ71C24

The AJ71C24 checks the control code received. It is not possible to read the control code from a sequence program.

(2) Data length

Data length expresses the number of bytes or words of data in the data area in 2-byte binary data. Data length units are determined according to the setting at address 103H of the buffer memory.

(a) Data send from an AJ71C24 to a computer

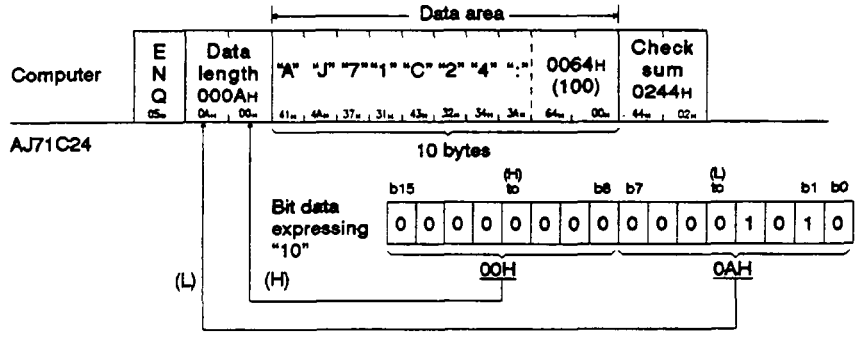
The data length to be transmitted is the value written to the send data length storage area of the AJ71C24 buffer memory by the TO instruction in a sequence program.

The AJ71C24 transmits the written value as it is from the lower byte (L).

(b) Data send from a computer to an AJ71C24

The AJ71C24 checks the received data length. When it is correct, the AJ71C24 writes the first 1 byte to the lower byte position (L) of the received data length storage area of the AJ71C24 buffer memory.

Example: Data length when transmitting "AJ71C24:" and value "100" (units: bytes)



(3) Data area

The data of 00H to FFH code can be processed in a string of 1-byte data as the send data.

(a) Data send from an AJ71C24 to a computer

The data area to be transmitted is the value written to the send data storage area of the AJ71C24 buffer memory by the TO instruction in a sequence program.

The AJ71C24 transmits the data according to the designated length and byte/word units sequentially from the lower address in unchanged codes.

(b) Data send from a computer to an AJ71C24

The data area received is written to the received data storage area sequentially from the lower address in unchanged codes as they are received.

The data length to be written is determined by the data length in the received message and the designated word/byte units.

(4) Check sum

The check sum is the lower 2 bytes (16 bits) of the result obtained by adding the data length and the data area in the message as binary data.

If the setting at address 115H is "1", the check sum is not required.

(a) Data send from an AJ71C24 to a computer

The AJ71C24 calculates and adds the check sum.

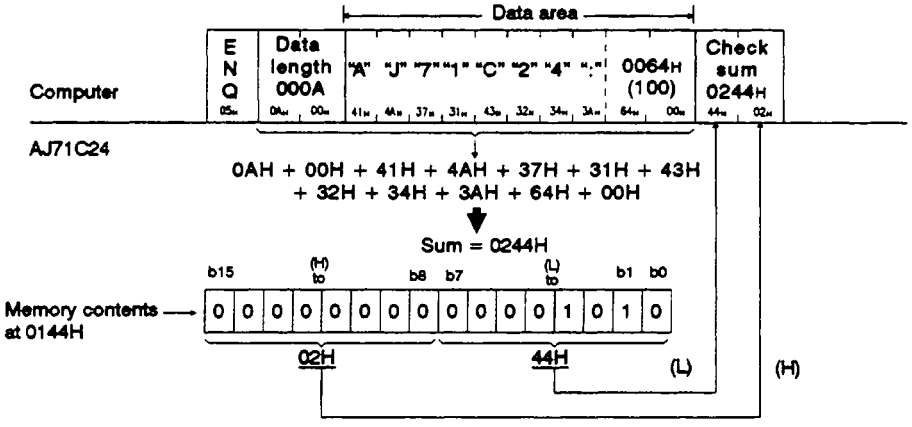
If the check sum is not processed, the check sum is not transmitted.

(b) Data send from a computer to an AJ71C24

The AJ71C24 checks and processes the check sum received. It is not possible to read the check sum from a sequence program.

When the setting is "check sum is disabled", the received data following the data of the designated length is ignored up to the next control code.

Example: Check sum when transmitting "AJ71C24:" and value "100" (units: bytes) is processed as follows.



(5) Error code

An error code indicates the error content when an NAK response is received. The code is transmitted and received in the range of 0001H to 00FFH. Section 11.2 gives error code details.

(a) Data send from an AJ71C24 to a computer

The AJ71C24 appends the error code.

When transmitting an error code, the AJ71C24 writes the same error code to its error code storage area in the received data buffer memory area.

(b) Data send from a computer to an AJ71C24

The AJ71C24 writes the received error code to the error code storage area in its send data buffer memory area.

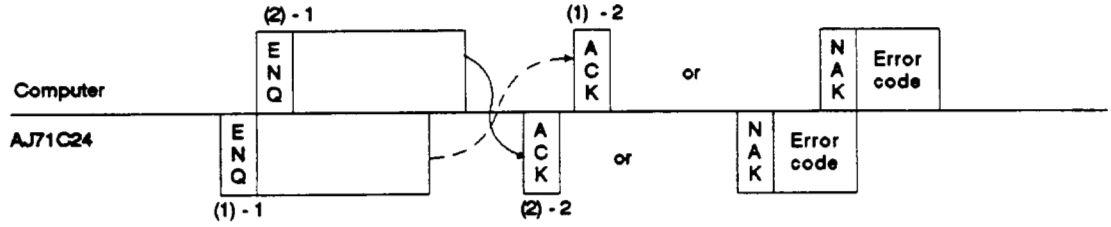
POINT

In bidirectional communications, check sum and error codes are all binary data. Note that in the dedicated protocol, they are handled in ASCII code.

10.6 Processing an AJ71C24 for Simultaneous Send in Full-Duplex Mode

Processing by the AJ71C24 varies depending on the setting (valid/invalid setting at simultaneous transmission) when the computer and the AJ71C24 transmit data at the same time to each other.

Example:



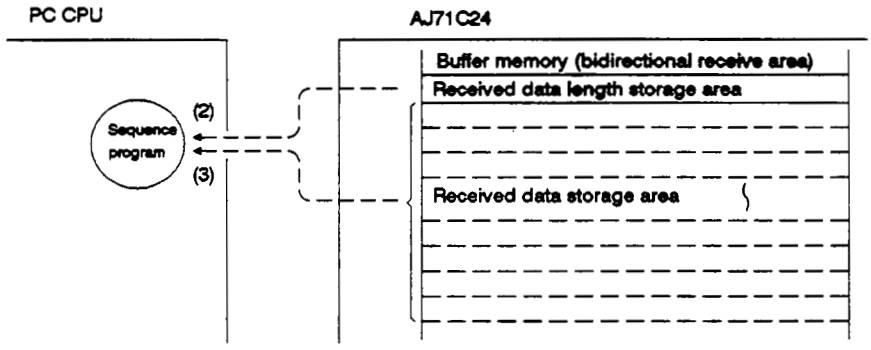
Buffer Memory Setting (Address 114H)	Setting	Processing by AJ71C24	
		Send Processing	Receive Processing
0000H	Send data : Valid Received data : Valid	After completing data send ((1)-1), the AJ71C24 waits for response ((1)-2) while checking time-out error. Normal or abnormal send completion is confirmed by response and its status is transmitted to the sequence program via the buffer memory.	After completing data receive ((2)-1), the AJ71C24 transmits the response ((2)-2). The received data and receive result are transmitted to the sequence program via the buffer memory.
0100H	Send data : Invalid Received data : Valid	After completing data send ((1)-1), the AJ71C24 transmits the sequence program of a simultaneous transmission error (error code: 3) via the buffer memory. The AJ71C24 does not wait for a response ((1)-2).	After completing data receive ((2)-1), the AJ71C24 transmits the response ((2)-2). The receive data and receive result are transmitted to the sequence program via the buffer memory.
0001H	Send data : Valid Received data : Invalid	After completing data send ((1)-1), the AJ71C24 waits for a response ((1)-2) while checking time-out error. Normal or abnormal send completion is confirmed by a response and its status is transmitted to the sequence program via the buffer memory.	Data receive ((2)-1) is ignored and received data is discarded. The response ((2)-2 is not transmitted. Data receive is not transmitted to the sequence program.
0101H	Send data : Invalid Received data : Invalid	After completing data send ((1)-1), the AJ71C24 transmits the sequence program of a simultaneous transmission error (error code: 3) via the buffer memory. The AJ71C24 does not wait for a response ((1)-2).	Data receive ((2)-1) is ignored and received data is discarded. The response ((2)-2 is not transmitted. Data receive is not transmitted to the sequence program.

10.7 Basic Program to Read/Write Buffer Memory

The following describes a basic sequence program to bidirectional read and write data to and from the AJ71C24 buffer memory.

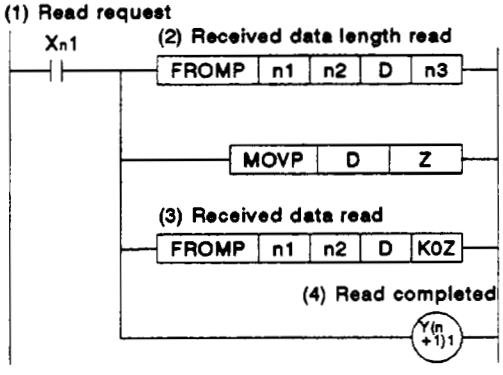
(1) Reading data from the receive area (FROM, FROMP, DFRO, DFROP)

Data is read from the buffer memory bidirectional receive area (default: 80H to FFH).



Format

(1) Read request



Reads the received data length from the no-protocol received data length storage area of buffer memory when the read request signal (Xn1) is turned ON.

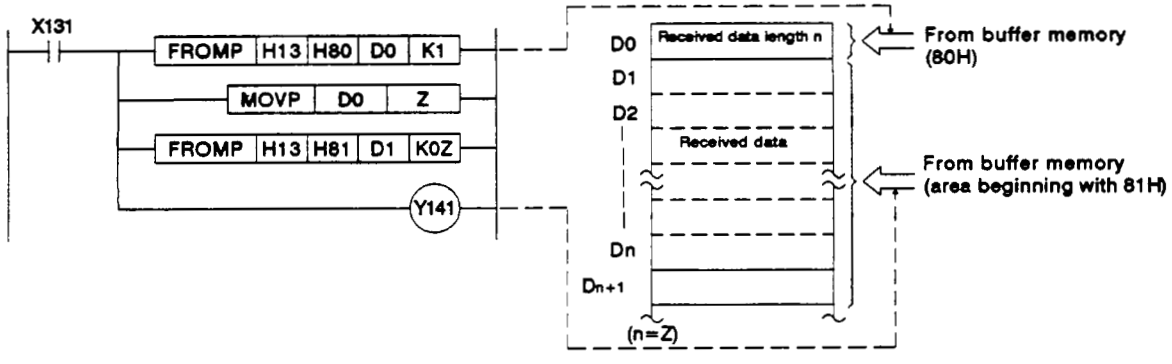
Stores the read data length to the index register (Z).

Reads the received data of the read received data length from the received data storage area of buffer memory.

Turns ON the read completed signal (Y(n+1)1) after the recieved data has been read

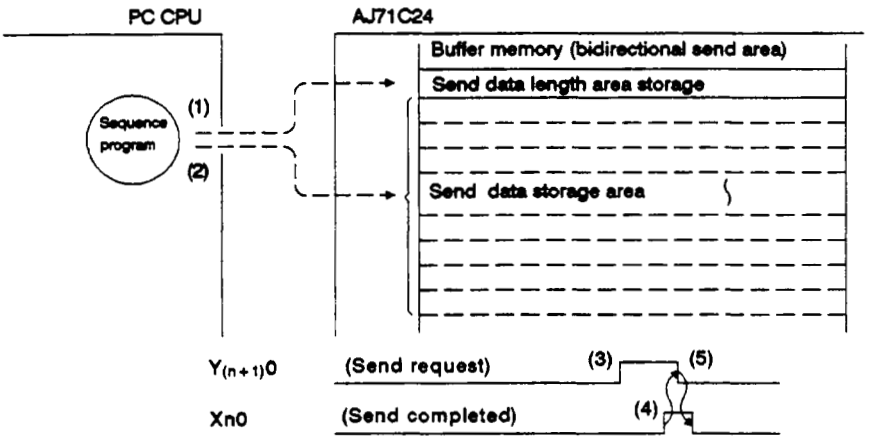
* Data read by program (3) is processed as the recieved data.

Example: To read the data of (n+1) words from the area, beginning with buffer memory address 80H, to the area beginning with D0 when the AJ71C24 I/O numbers are allocated to 130 to 14F (unit: word).

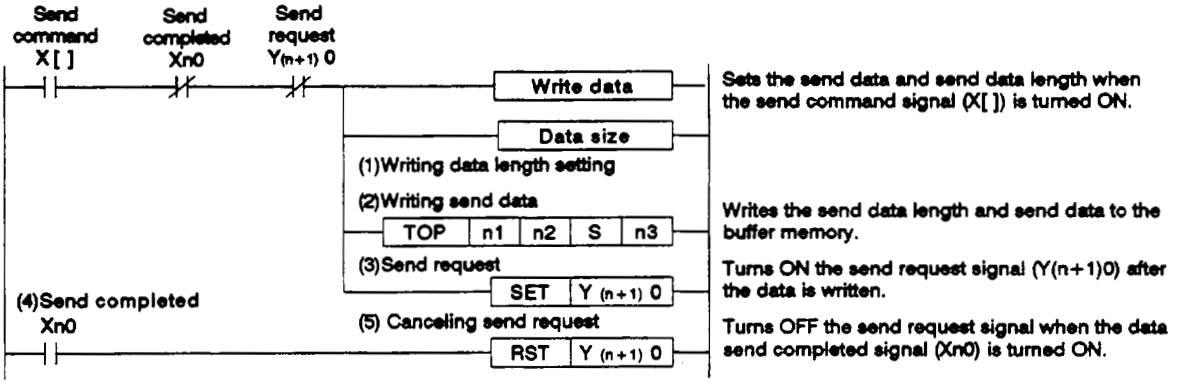


(2) Writing data to the send area (TO, TOP, DTO, DTOP)

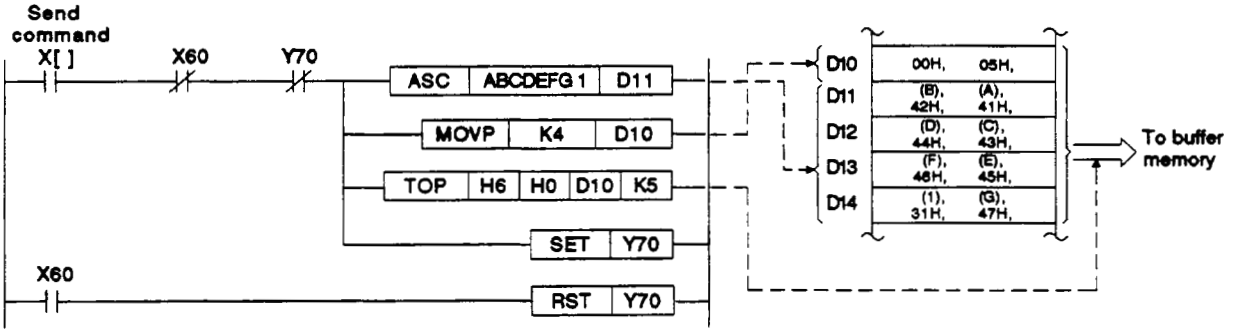
Data written to the bidirectional send area (default: 0H to 7FH).



Format


Send command X[ ]
Send completed Xn0
Send request Y(n+1) 0
Write data
Data size
(1)Writing data length setting
(2)Writing send data
TOP n1 n2 S n3
(3)Send request
SET Y (n+1) 0
(4)Send completed Xn0
(5) Canceling send request
RST Y (n+1) 0
Sets the send data and send data length when the send command signal (X[ ]) is turned ON.
Writes the send data length and send data to the buffer memory.
Turns ON the send request signal (Y(n+1)0) after the data is written.
Turns OFF the send request signal when the data send completed signal (Xn0) is turned ON.

Example: To transmit 4-word data after writing "ABCDEFG1" to the buffer memory area from 1H when the AJ71C24 I/O numbers are allocated to 60 to 7F.



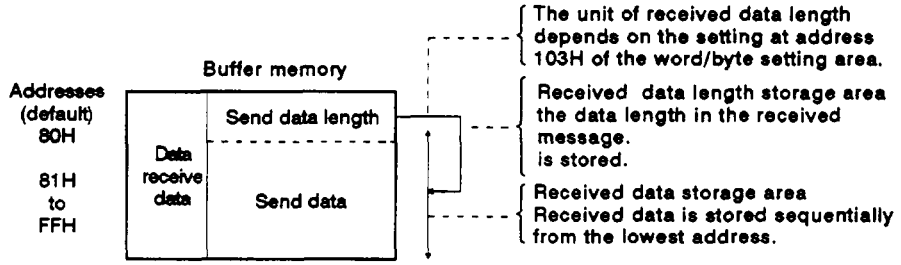
10.8 Receiving Data in the Bidirectional Mode (Computer → AJ71C24)

(1) Data receive area

The AJ71C24 stores the received data length and the received data in the data receive area.

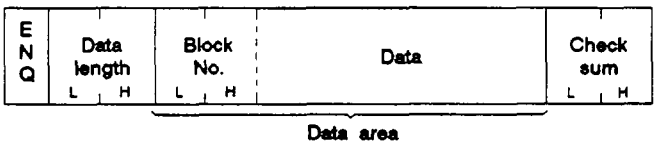
With a default setting, 80H to FFH in the buffer memory is allocated as the data receive area.

This area may be changed as needed. Section 7.4.5 gives procedure for changing the data receive area.


Buffer memory
Addresses (default)
80H
81H to FFH
Send data length
Data receive data
Send data
The unit of received data length depends on the setting at address 103H of the word/byte setting area.
Received data length storage area the data length in the received message. is stored.
Received data storage area Received data is stored sequentially from the lowest address.

If the length of the data area in the message transmitted from the computer is greater than the received data storage area (default: 127 words), split the data area into several blocks so that its length is smaller than the received data storage area and append the block number to specify each data area block.

Message format example:



(2) Reading received data

The AJ71C24 makes a read request to the PC CPU at the following timing (the timing at which the X1A1 signal in the program example in (4) is turned on).

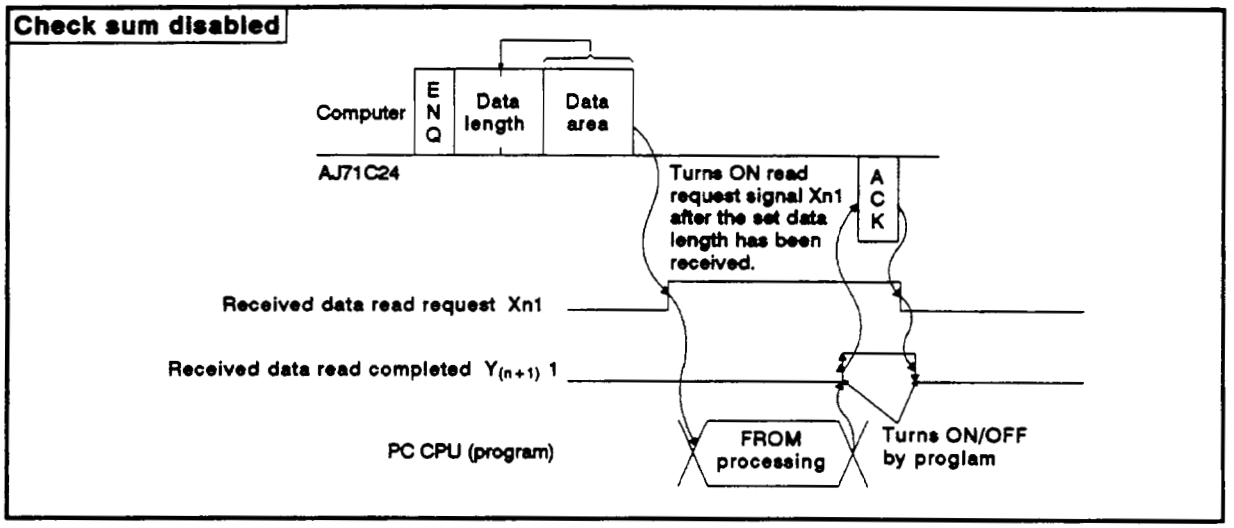
- When the data length in the message and the set data length (bytes or words as set in address 103H) have been received.
- If the check sum is processed, when the check sum has been received with the above mentioned data area.

Example:

Word/byte setting: Word units
Data length in message: 10
In this case, the AJ71C24 makes a read request to the the sequence program at the time 10 words of data (plus the check sum) have been received.

When the read request (Xn1) for the received data is made read the data length and that length of data with a FROM instruction in a sequence program and turn OFF the received data read completed signal (Y (n+1)1).

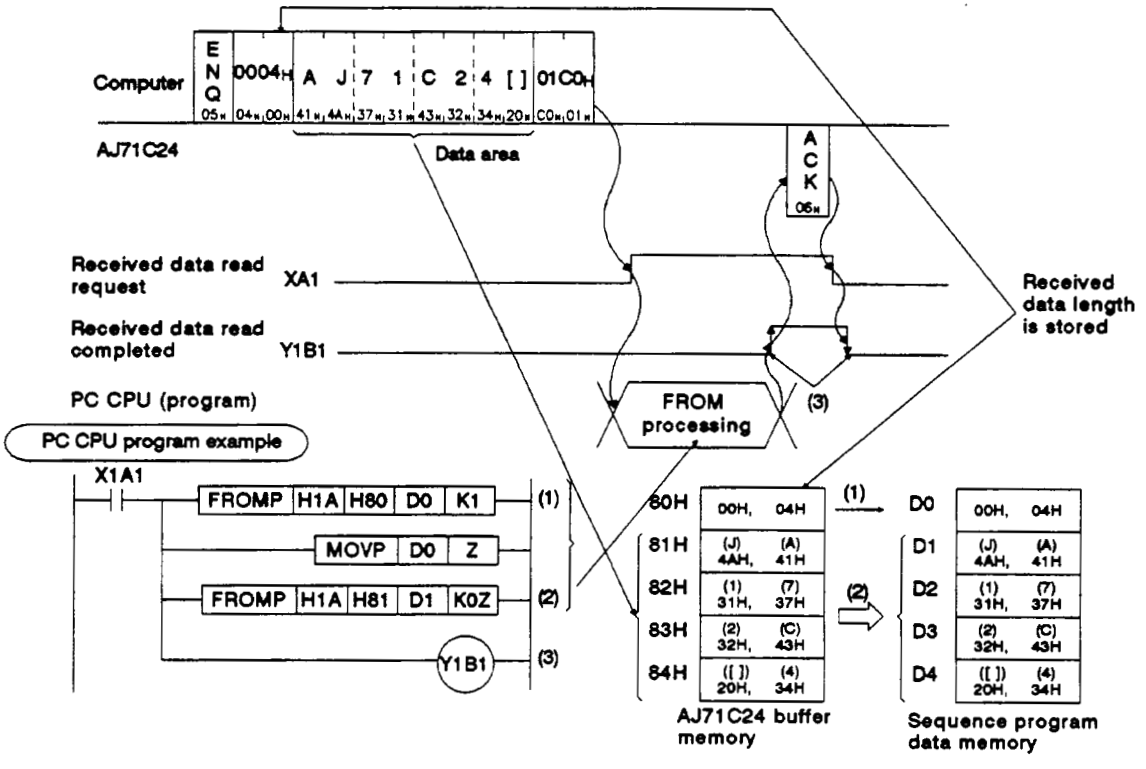
(3) Data receive processing



(4) Data receive program examples

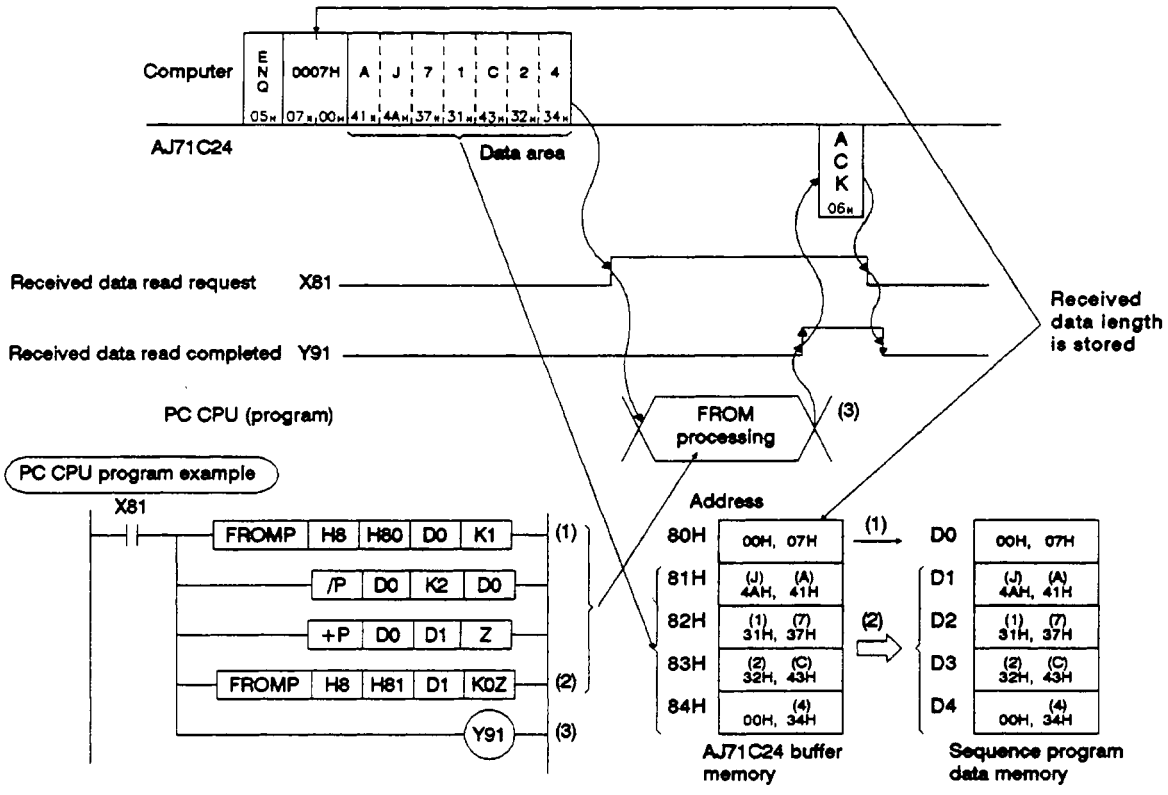
Example 1 Check sum enabled, in word units (buffer memory area allocation: default)

To store "AJ71C24 [ ]", received from a computer, to D0 to D4 of a PC CPU.
(AJ71C24 I/O address: 1A0 to 1BF)



Example 2 Check sum disabled, in byte units (receive memory area allocation: default)

To store "AJ71C24", received from a computer, to D0 to D4 of a PC CPU. (AJ71C24 I/O address: 80 to 9F)



POINT

- Even if send data units are set to byte units, the FROM instruction in a sequence program operates in word units. Therefore, the received data length must be converted to the number of buffer memory points (word units).
  In the above example, 7 bytes of data must be converted into 4 words (7 ÷ 2 = 3.5).
- When an odd number of bytes of data is received, the higher 8 bits of the last address read by the FROM instruction are "00H".

10.9 Transmitting Data in the Bidirectional Mode (AJ71C24 → Computer)

Transmitting means outputting data which was written to the bidirectional mode send buffer memory area (hereafter referred to as the send area), from the AJ71C24 to a computer in response to turning ON the PC CPU send request signal (Y(n+1)0).

(1) Send area and writing send data

The send data length and send data are written to the send area.

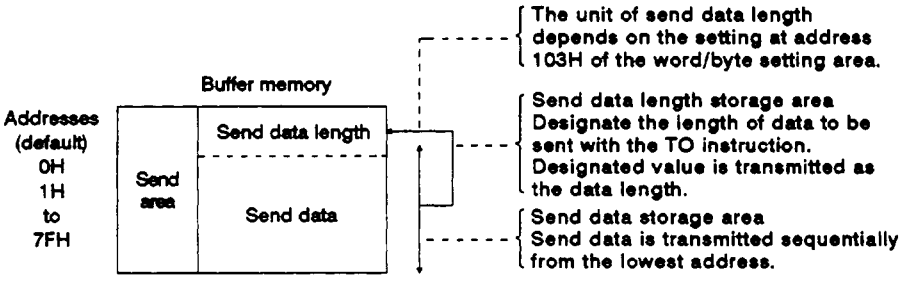
(a) The length of data to be written (having been written) to the bidirectional send data length storage area in either words or bytes.

(b) The data to be transmitted is written to the send data storage area.

When the send request signal (Y(n+1)0) is turned ON after (a) and (b) have been executed, the AJ71C24 transmits the designated length of designated data from the send data storage area sequentially from the lower address.

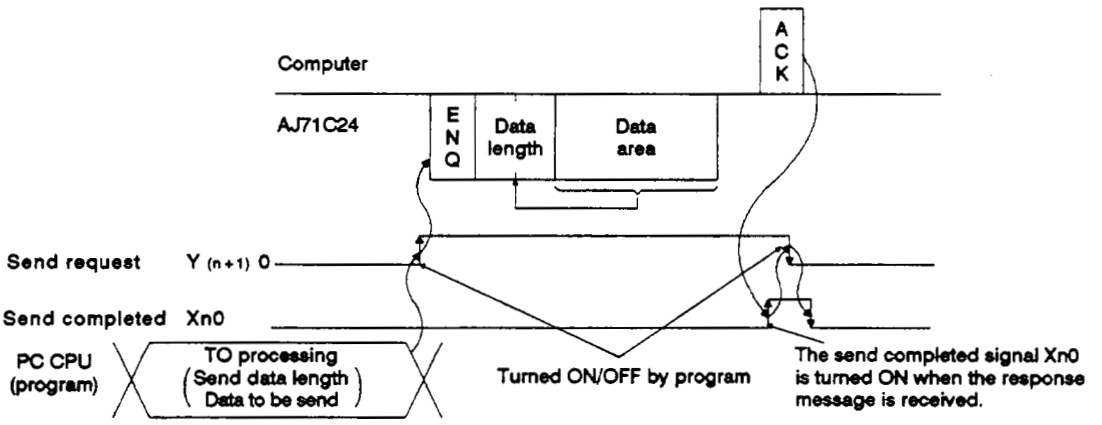
By default, the buffer memory area 0H to 7FH is allocated to the send area.

This area may be changed as needed. Section 7.4.4 gives the procedure for changing the send area addresses.


Buffer memory
Addresses (default)
0H
1H
to
7FH
Send area
Send data length
Send data
The unit of send data length depends on the setting at address 103H of the word/byte setting area.
Send data length storage area
Designate the length of data to be sent with the TO instruction.
Designated value is transmitted as the data length.
Send data storage area
Send data is transmitted sequentially from the lowest address.

(2) Data transmitting procedure

Procedure (Check sum disabled)



POINTS

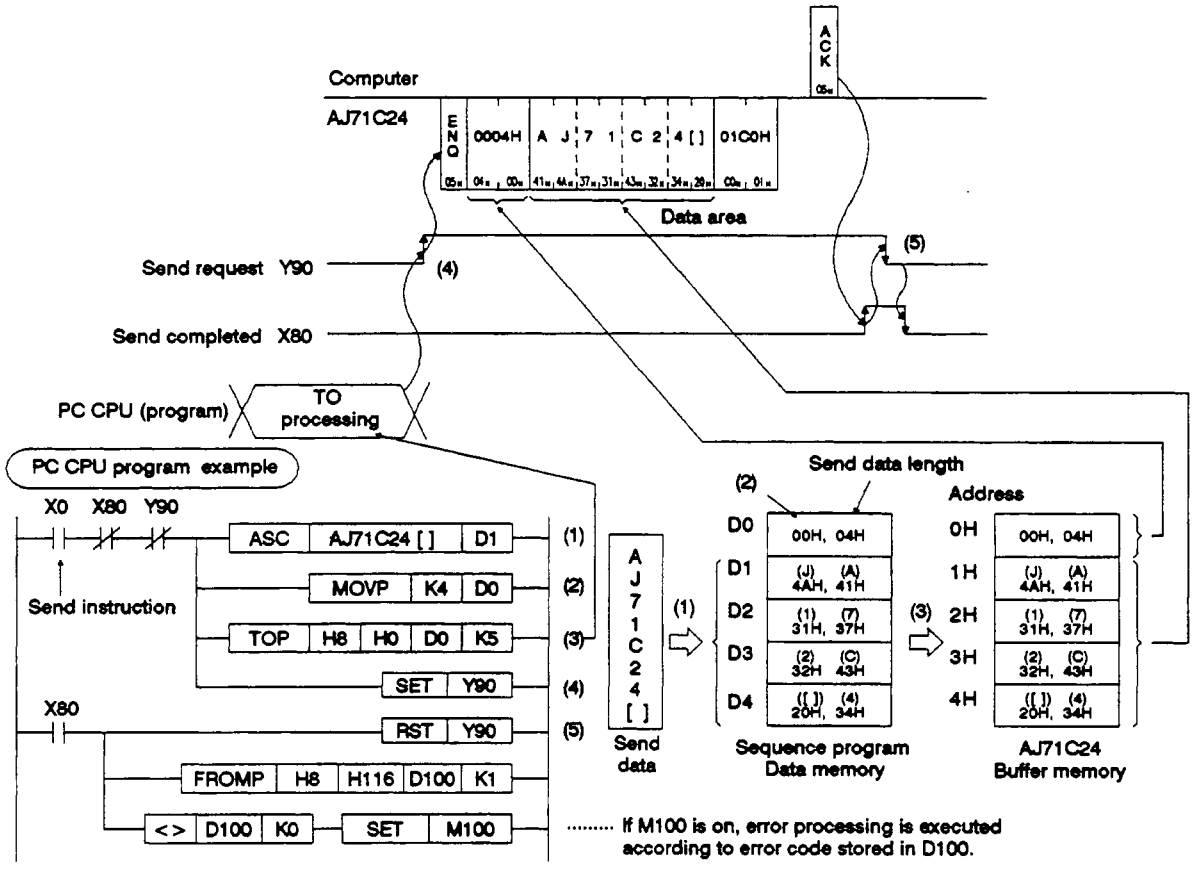
(1) An error occurs if the send data length is (a) greater than the send area, or (b) equal to "0". In this case, "1" is written as send error information to the most significant bit (bit 15) of address 116H (data send error storage area) in the special applications memory area (see Sections 10.2 and 11.2).

(2) The send data length written to the head address is transmitted as the data length.

(3) Transmission program examples

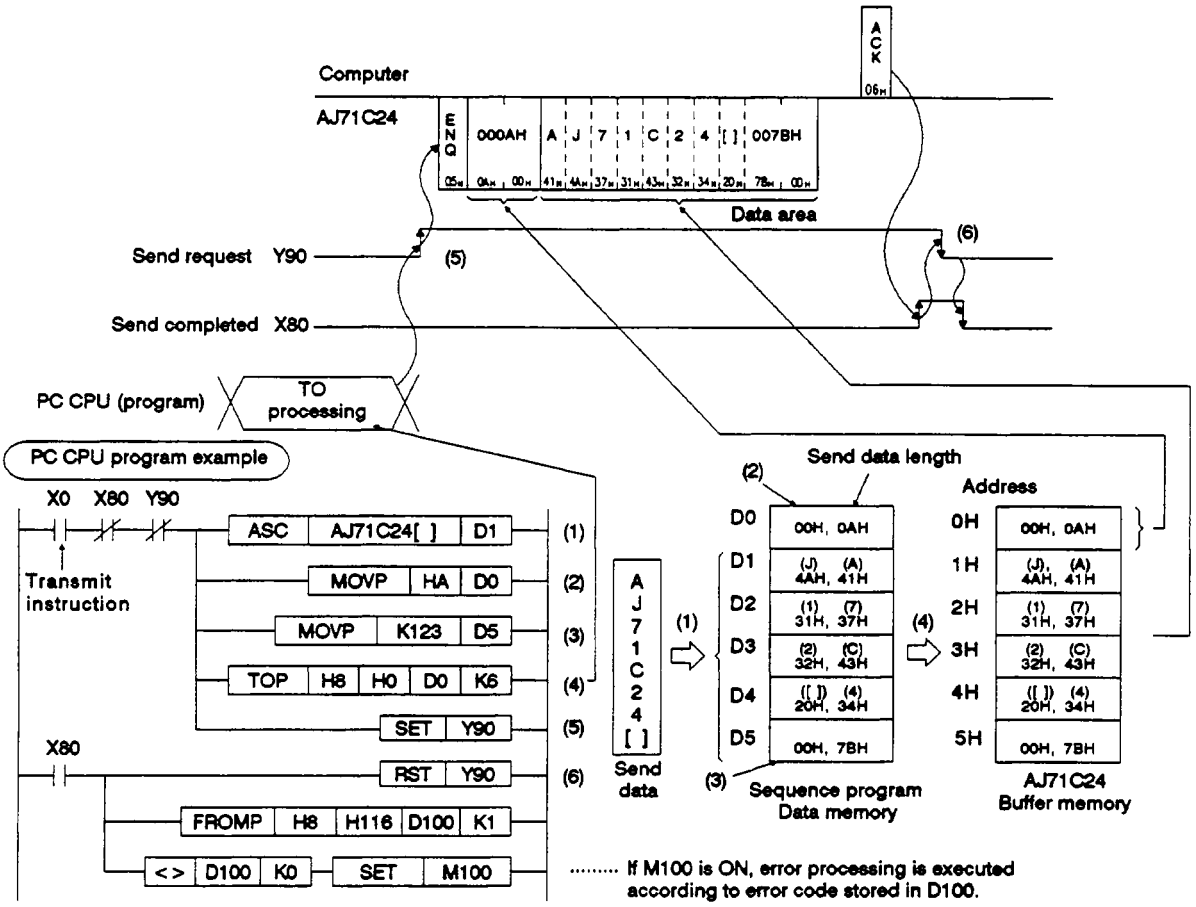
Example 1 Check sum enabled, in word units (buffer memory area allocation: default)

To transmit "AJ71C24 [ ]" from the PC CPU to a computer after writing it to buffer memory. (AJ71C24 I/O address: 80 to 9F)



Example 2 Check sum disabled, in byte units (send data area allocation: default)

To transmit character data "AJ71C24 [ ]" and integer data "123" (decimal) from the PC CPU to a computer after writing it to buffer memory. (AJ71C24 I/O address: 80 to 9F)



POINT

- Even if send data units are set to byte units, the TO instruction in a sequence program operates in word units. Therefore, the length of send data differs from the data length designated by the TO instruction.

11. TROUBLESHOOTING

This chapter describes errors which can occur with the AJ71C24 procedures.

11.1 NAK Error Codes with Dedicated Protocols

Table 11.1 gives the error codes and their descriptions when the NAK code is transmitted between the computer and the PC CPU as 2-digit ASCII (hexadecimal) between 00H and FFH.
If several errors occur simultaneously, the code with the lowest number takes precedence and is transmitted.
If any of the following errors occur, the transmission sequences are initialized and LEDs 2-N3U and 4-NEU (LED Nos. 4 and 7) are turned ON.

Table 11.1 Error Code List

Error Code (Hexadecimal)	Error	Error Description	Indicator LED No.	Corrective Actions
00H	Disable during RUN	Invalid access has been made during RUN. (1) Data has been written to a PC CPU with the SW22 OFF (write disable during RUN). (2) Sequence program and parameters have been written.	2-C/N (LED No.16) 4-C/N (LED No.20)	(1) Start communicationss after turning ON SW22. (2) Write parameters after setting the PC CPU to STOP.
01H	Parity error	Parity error With the SW16 ON (parity enabled), the parity check result does not match the state of SW17 (odd/even parity).	2-P/S (LED No.17) 4-P/S (LED No.21)	Check control protocol, change the SW setting or data.
02H	Sum check error	Sum check error With the SW21 ON (sum check enabled), the sum check result of received data does not match the sum check code of transmitted data, i.e., send data is different from received data.	2-P/S (LED No.17) 4-P/S (LED No.21)	Check data transmitted from computer and sum check result. Correct invalid data.
03H	Protocol error	Communications protocol not valid. Communications have been made with a protocol different from the one set by the mode setting switch.	2-PRO (LED No.18) 4-PRO (LED No.22)	Check and correct the mode setting switch position and control protocol and restart data communications.
04H	Framing error	Framing error Data does not match the setting of SW18 (stop bit).	2-SIO (LED No.19) 4-SIO (LED No.23)	Change the setting of SW18 or the control protocol.
05H	Overrun error	Overrun error New data has been transmitted before AJ71C24 receives all the preceding data.	2-SIO (LED No.19) 4-SIO (LED No.23)	Decrease the data transmission speed and restart data communications.
06H	Character area error	Character area A, B, or C error, or designated command does not exist. (1) The designation of the character area A, B, or C for the control protocol set with the mode setting switch is not correct. (2) A command used with the protocol does not exist. The number of processing points is outside the allowable range, or the designated device number does not exist in the designated PC CPU. The set device number does not exist in the set PC CPU. (3) The device number is not set with the required number of characters. (ACPU common command: 5 characters, AnACPU dedicated command: 7 characters)	2-PRO (LED No.18) 4-PRO (LED No.22)	(1) Check and correct the character area A,B, or C and restart data communications. (2) See the functions list in Section 3.3.1 and the ACPU User's Manual to correct the designated commands, and restart data communications. (3) See Section 8.7.1 to correct the number of setting characters of the device number, and restart data communications.

Error Code (Hexadecimal)	Error	Error Description	Indicator LED No.	Corrective Actions
07H	Character error	Character error received. A character other than "A to Z", "0 to 9", "_" and control codes in Section 8.4.5 (1) has been	2-PRO (LED No.18) 4-PRO (LED No.22)	Check and correct data.
08H	PC CPU access error	Buffer memory is unable to make communications with the PC CPU. The PC CPU is not the type mentioned in Section 2.2.	2-C/N (LED No.16) 4-C/N (LED No.20)	Use a PC CPU which can perform data communications.
10H	PC CPU number error	Defined PC CPU number does not exist. The PC CPU number designated with the protocol was not the self (FFH) or a station number set with the MELSECNET link parameters.	2-C/N (LED No.16) 4-C/N (LED No.20)	Change the PC CPU number to the self (FFH) or a station number set with the MELSECNET link parameters, and restart data communications.
11H	Mode error	Incorrect communications between an AJ71C24 and a PC CPU. After the AJ71C24 has correctly received a request from the computer, normal data communications is not performed between the AJ71C24 and PC CPU due to noise or some other reason.	—	Restart data communications. If the error recurs, (a) check for noise and/or other causes, or (b) replace the AJ71C24. Restart data communications.
12H	Special function module designation error	Special function module designation error. A special function module, having buffer memory and capable of performing data communications, is not placed in the designated special function module number's position. Or the module number is wrong.	2-C/N (LED No.16) 4-C/N (LED No.20)	Check control protocol data or change the special function module location.
13H	Program step number designation error	Error in the designation of a sequence program step number. (1) A step number was designated which lies outside the program range designated by the PC CPU parameters. (2) A subsequence program that does not exist (or cannot be designated) was designated.	2-PRO (LED No.18) 4-PRO (LED No.22)	(1) Designate a step number which lies within the designated range, or change the parameters and restart transmission. (2) Check the model name and the set parameter values of the corresponding PC CPU.
18H	Remote error	Remote RUN/STOP impossible. Remote STOP/PAUSE has already been executed from another module (such as another AJ71C24).	2-PRO (LED No.18) 4-PRO (LED No.22)	Check for and reset remote STOP/PAUSE from another module.
20H	Data link error	Access was made to a station with which communications has been discontinued.	2-C/N (LED No.16) 4-C/N (LED No.20)	Check the state of data link.
21H	Special function module bus error	Memory access to the special function module cannot be made (for command TR, TW). (1) Special function module control bus error. (2) Special function module breakdown.	2-C/N (LED No.16) 4-C/N (LED No.20)	PC CPU, base unit, special function module or AJ71C24 hardware fault. Consult the nearest Mitsubishi representative.

REMARK

(1) Error codes 00H to 08H are transmitted to a computer after diagnosis by an AJ71C24, when access is made by the computer to the AJ71C24.

(2) Error codes 10H to 21H are transmitted from an AJ71C24 to a computer after diagnosis by a PC CPU when access is made by an AJ71C24 to the PC CPU.

11.2 Bidirectional Mode Error Codes

Table 11.2 gives the error codes, error descriptions, and corrective actions for errors which may occur during bidirectional mode communications.

The following error codes (1-word integers) are transmitted in order of the lower byte and the higher byte immediately following the NAK code when an error has occurred. (e.g., when the error code is 01_H, 01_H is transmitted first, and then 00_H is transmitted.)

Table 11.2 Error Code List

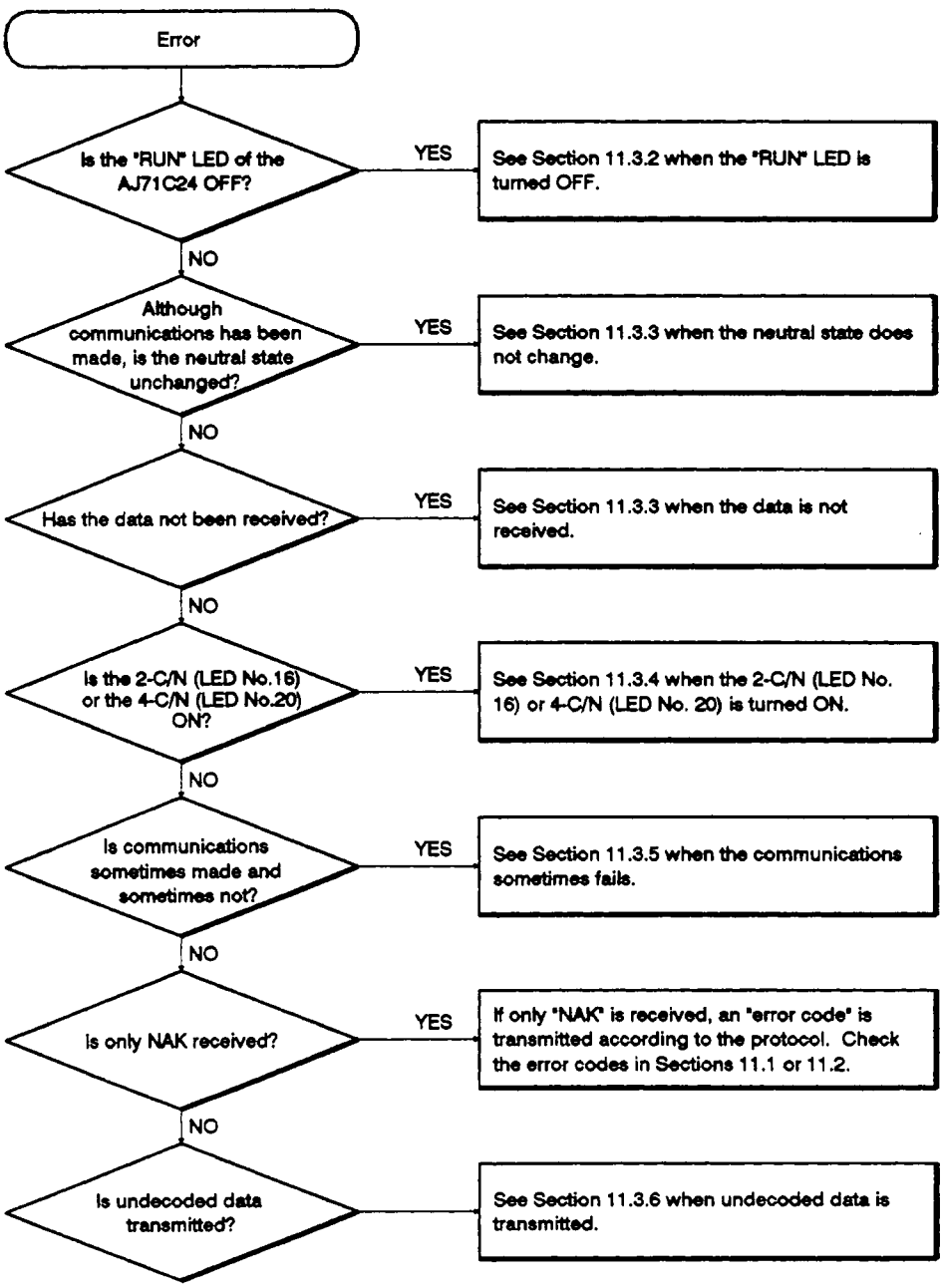
Error Code (Hexadecimal)	Error Descriptions	Corrective Actions
01H	Send data length error	Either (a) make the setting size of the send data length storage area in the buffer memory for bidirectional transmission smaller than the size of the send data storage area, or (b) set the send data length to "1" or greater. (Data which does not have a data part cannot be transmitted using the bidirectional mode.)
02H	Response message time-out error	Set the computer so that it transmits the response message (in response to the data received from the AJ71C24) to the AJ71C24 within the set value of the time-out time setting area (address 113H) in the AJ71C24 buffer memory.
03H	Simultaneous transmission error	Either (a) interlock the computer with the AJ71C24 so that they cannot begin transmitting data simultaneously to each other, or (b) set the data valid/invalid setting area (address 114H) in the AJ71C24 buffer memory to "valid".
10H	Error code is not received when the NAK code is received	When the computer transmits the NAK code to the AJ71C24 in response to the data received from the AJ71C24, an error code should be added immediately after the NAK code.
22H~5FH	Errors designated by the user	These error codes are added to immediately after the NAK code. Take corrective actions according to the procedure fixed by user.
80H	SIO error at data receive Framing error Overrun error	• Transmit data from the computer according to the following settings with the AJ71C24 (see Section 4.3.2 for SW12 to SW18). • Data bit length with SW12 • Transmission speed with SW13 to SW15 • Stop bit length with SW18 • Use insulation transformers (noise-cutting transformers) to eliminate noise.
81H	Check sum error Parity error (only at data receive)	• To transmit the check sum to the AJ71C24, obtain the check sum as described in Section 10.5.2. Set the check sum enable/disable setting area (address 115H) in the AJ71C24 buffer memory to "disable", so that the check sum is not transmitted. • Transmit data from the computer according to settings with SW16 and SW17 of the AJ71C24.
83H	Received data length error	Either (a) make the data part length and the set value of the data part length of the receive message less than the size of the received data storage area, or (b) transmit correctly the data length (0001H or more) contained in the message which is transmitted to the AJ71C24. (Data which does not have the data part cannot be transmitted using the bidirectional mode.)
83H	Received data time-out error	When data is transmitted from the computer, set the actual length of the data part to the data length part. (The AJ71C24 executes the time-out check (as set with address 113H of the buffer memory) if it fails to receive data of a set length. This error occurs when it fails to receive the next data within the set time.)

11.3 Troubleshooting OFF

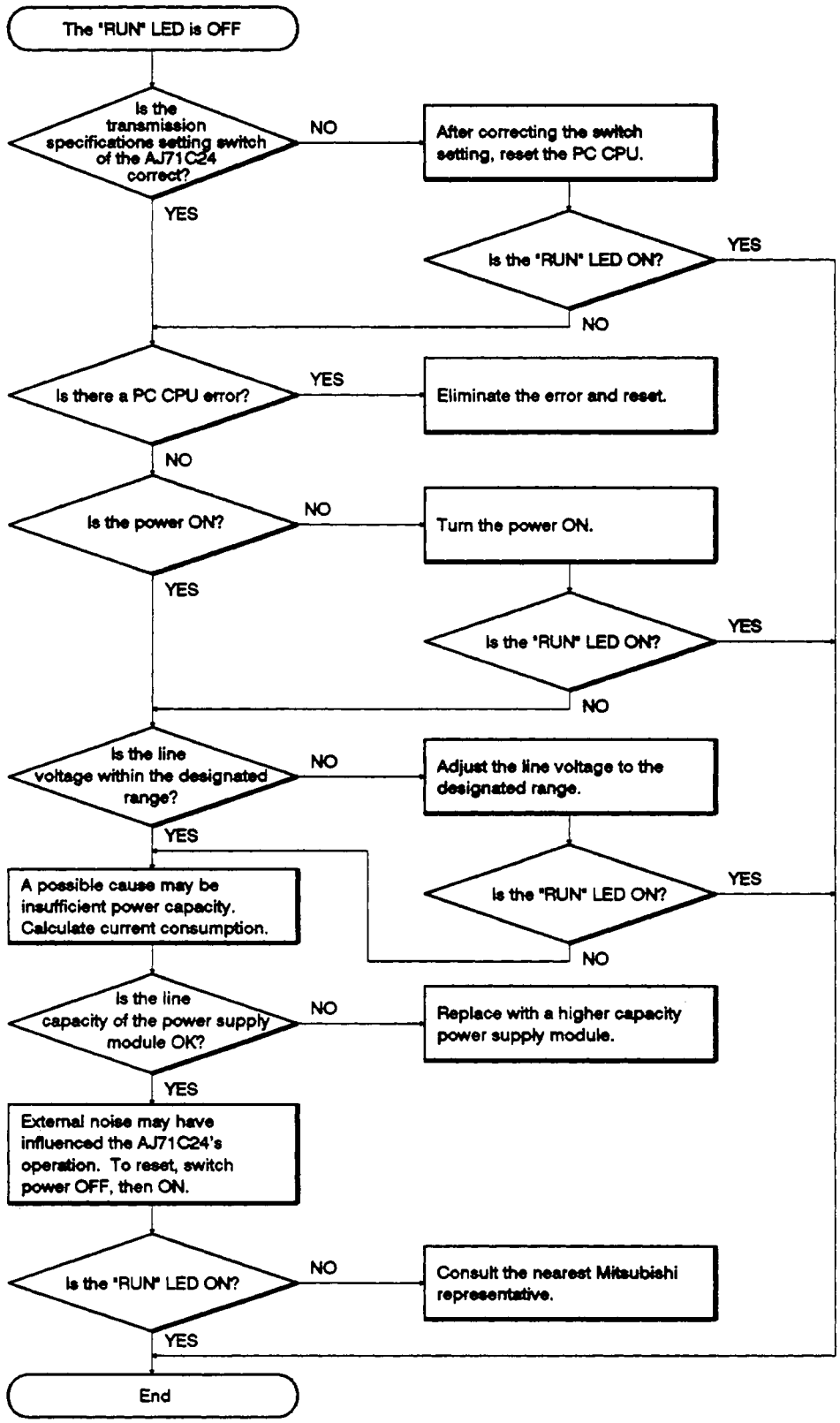
This section describes basic troubleshooting procedures for the AJ71C24. The User's Manuals give information on PC CPU module troubleshooting.

11.3.1 Troubleshooting flow chart

The state of errors is described as follows:

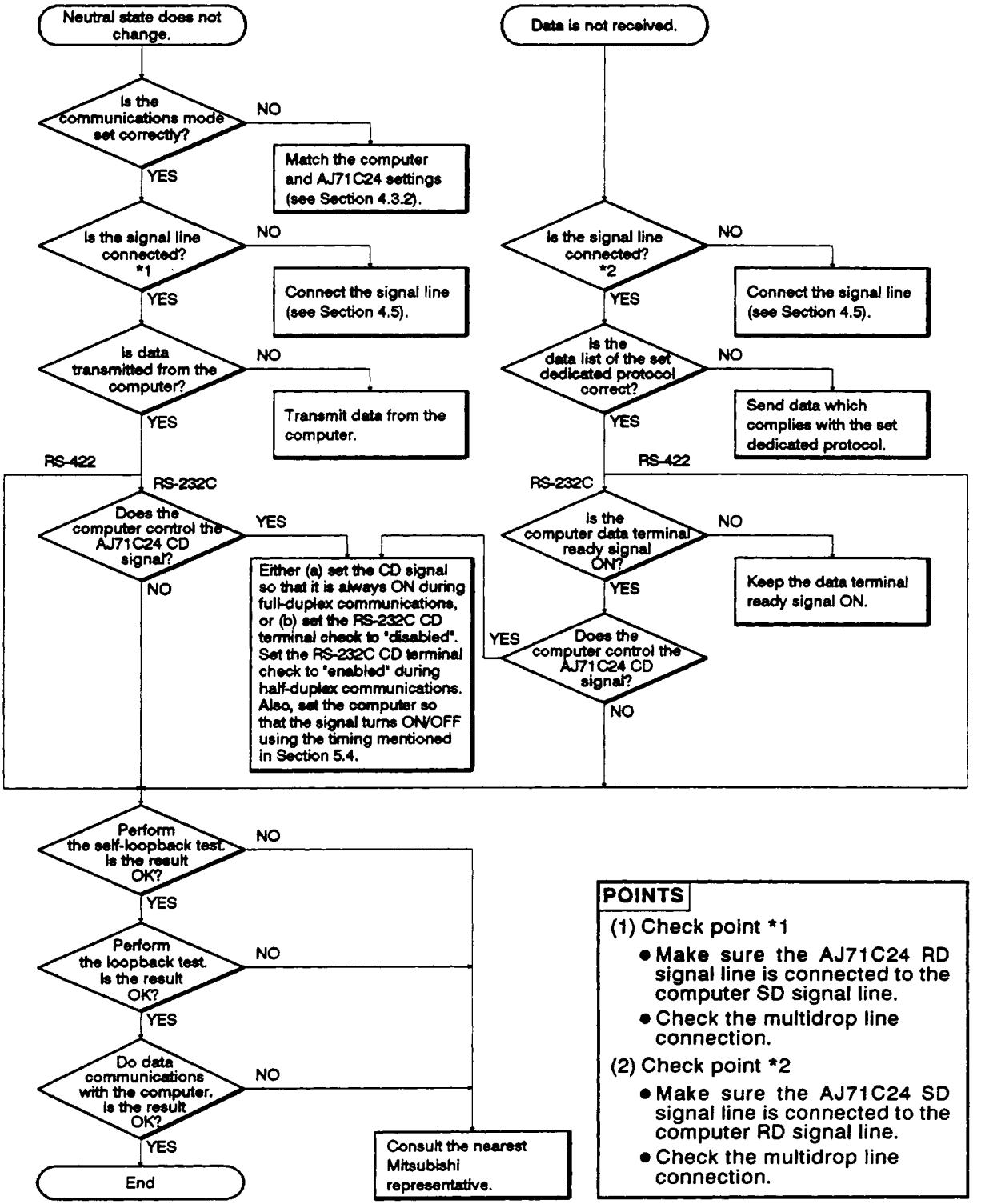

Error
Is the "RUN" LED of the AJ71C24 OFF?
YES
See Section 11.3.2 when the "RUN" LED is turned OFF.
NO
Although communications has been made, is the neutral state unchanged?
YES
See Section 11.3.3 when the neutral state does not change.
NO
Has the data not been received?
YES
See Section 11.3.3 when the data is not received.
NO
Is the 2-C/N (LED No.16) or the 4-C/N (LED No.20) ON?
YES
See Section 11.3.4 when the 2-C/N (LED No. 16) or 4-C/N (LED No. 20) is turned ON.
NO
Is communications sometimes made and sometimes not?
YES
See Section 11.3.5 when the communications sometimes fails.
NO
Is only NAK received?
YES
If only "NAK" is received, an "error code" is transmitted according to the protocol. Check the error codes in Sections 11.1 or 11.2.
NO
Is undecoded data transmitted?
See Section 11.3.6 when undecoded data is transmitted.

11.3.2 When the "RUN" LED is turned OFF


The "RUN" LED is OFF
Is the transmission specifications setting switch of the AJ71C24 correct?
NO
After correcting the switch setting, reset the PC CPU.
YES
Is the "RUN" LED ON?
YES
NO
Is there a PC CPU error?
YES
Eliminate the error and reset.
NO
Is the power ON?
NO
Turn the power ON.
YES
Is the "RUN" LED ON?
YES
NO
Is the line voltage within the designated range?
NO
Adjust the line voltage to the designated range.
YES
A possible cause may be insufficient power capacity. Calculate current consumption.
Is the "RUN" LED ON?
YES
NO
Is the line capacity of the power supply module OK?
NO
Replace with a higher capacity power supply module.
YES
External noise may have influenced the AJ71C24's operation. To reset, switch power OFF, then ON.
Is the "RUN" LED ON?
NO
Consult the nearest Mitsubishi representative.
YES
End

11.3.3 When the neutral state does not change or data is not received

The AJ71C24 LED remains ON indicating (a) the neutral state, or (b) that communications is disabled (even though a communications request is made to the AJ71C24). The computer cannot receive data.


Neutral state does not change.
Is the communications mode set correctly?
NO
Match the computer and AJ71C24 settings (see Section 4.3.2).
YES
Is the signal line connected? *1
NO
Connect the signal line (see Section 4.5).
YES
Is data transmitted from the computer?
NO
Transmit data from the computer.
YES
RS-422
RS-232C
Does the computer control the AJ71C24 CD signal?
YES
Either (a) set the CD signal so that it is always ON during full-duplex communications, or (b) set the RS-232C CD terminal check to "disabled". Set the RS-232C CD terminal check to "enabled" during half-duplex communications. Also, set the computer so that the signal turns ON/OFF using the timing mentioned in Section 5.4.
NO
Data is not received.
Is the signal line connected? *2
NO
Connect the signal line (see Section 4.5).
YES
Is the data list of the set dedicated protocol correct?
NO
Send data which complies with the set dedicated protocol.
YES
RS-422
RS-232C
Is the computer data terminal ready signal ON?
NO
Keep the data terminal ready signal ON.
YES
Does the computer control the AJ71C24 CD signal?
YES
NO
Perform the self-loopback test. Is the result OK?
NO
YES
Perform the loopback test. Is the result OK?
NO
YES
Do data communications with the computer. Is the result OK?
NO
YES
End
Consult the nearest Mitsubishi representative.

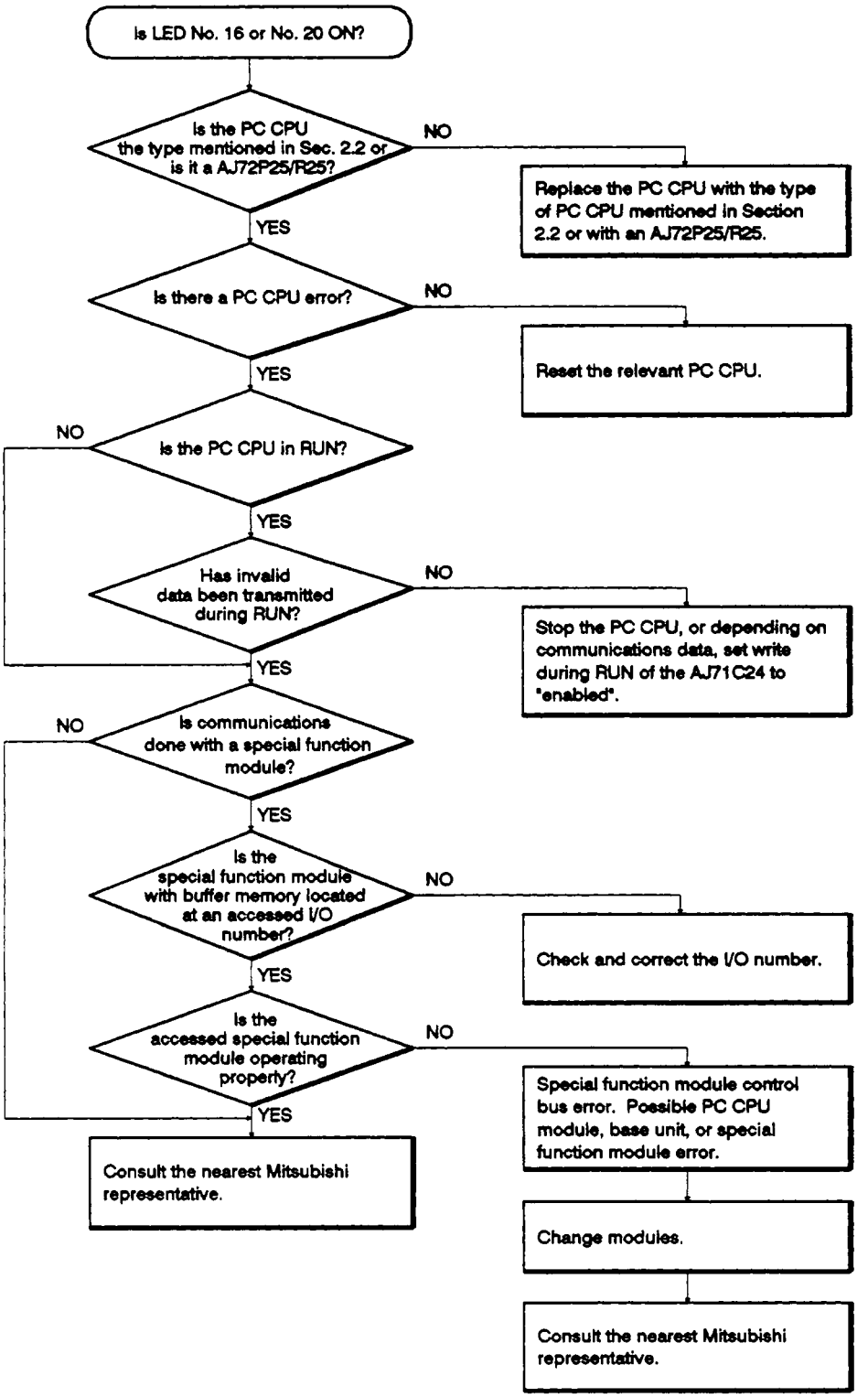
POINTS

(1) Check point *1
- Make sure the AJ71C24 RD signal line is connected to the computer SD signal line.
- Check the multidrop line connection.

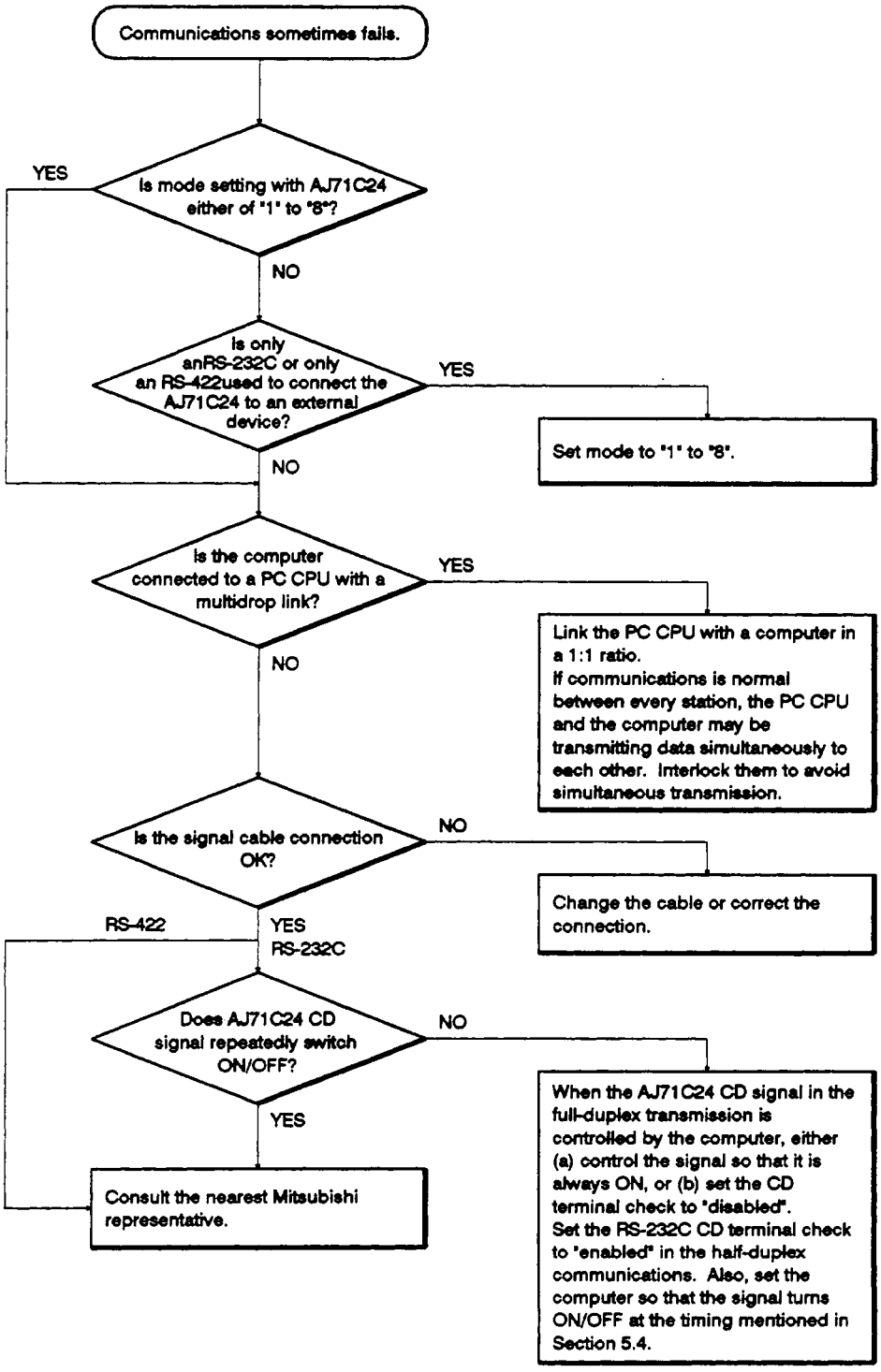
(2) Check point *2
- Make sure the AJ71C24 SD signal line is connected to the computer RD signal line.
- Check the multidrop line connection.

11.3.4 When the 2-C/N (LED No. 16) or 4-C/N (LED No. 20) is turned ON

Flow chart to use when the 2-C/N (LED No. 16) or 4-C/N (LED No. 20) on the AJ71C24 panel turns ON.

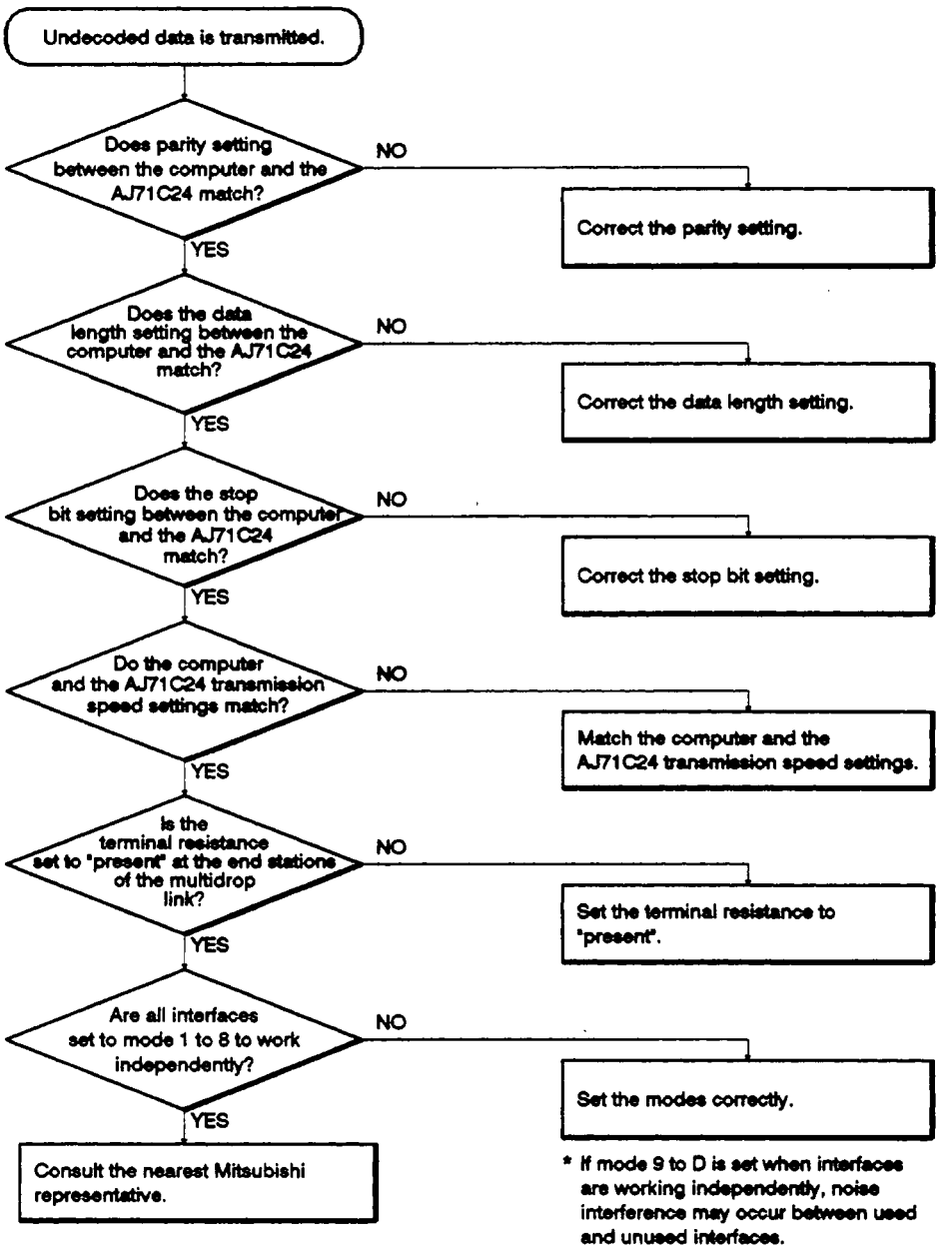

Is LED No. 16 or No. 20 ON?
Is the PC CPU the type mentioned in Sec. 2.2 or is it a AJ72P25/R25?
NO
Replace the PC CPU with the type of PC CPU mentioned in Section 2.2 or with an AJ72P25/R25.
YES
Is there a PC CPU error?
NO
Reset the relevant PC CPU.
YES
NO
Is the PC CPU in RUN?
YES
Has invalid data been transmitted during RUN?
NO
Stop the PC CPU, or depending on communications data, set write during RUN of the AJ71C24 to "enabled".
YES
NO
Is communications done with a special function module?
YES
Is the special function module with buffer memory located at an accessed I/O number?
NO
Check and correct the I/O number.
YES
Is the accessed special function module operating properly?
NO
Special function module control bus error. Possible PC CPU module, base unit, or special function module error.
YES
Consult the nearest Mitsubishi representative.
Change modules.
Consult the nearest Mitsubishi representative.

11.3.5 When communications sometimes fails


Communications sometimes fails.
Is mode setting with AJ71C24 either of "1" to "8"?
YES
NO
Is only anRS-232C or only an RS-422used to connect the AJ71C24 to an external device?
YES
Set mode to "1" to "8".
NO
Is the computer connected to a PC CPU with a multidrop link?
YES
Link the PC CPU with a computer in a 1:1 ratio.
If communications is normal between every station, the PC CPU and the computer may be transmitting data simultaneously to each other. Interlock them to avoid simultaneous transmission.
NO
Is the signal cable connection OK?
NO
Change the cable or correct the connection.
RS-422
YES
RS-232C
Does AJ71C24 CD signal repeatedly switch ON/OFF?
NO
When the AJ71C24 CD signal in the full-duplex transmission is controlled by the computer, either (a) control the signal so that it is always ON, or (b) set the CD terminal check to "disabled".
Set the RS-232C CD terminal check to "enabled" in the half-duplex communications. Also, set the computer so that the signal turns ON/OFF at the timing mentioned in Section 5.4.
YES
Consult the nearest Mitsubishi representative.

11.3.6 When undecoded data is transmitted

Use this flow chart when the AJ71C24 (in response to data from the computer) transmits code and data which is not included in the control code.


Undecoded data is transmitted.
Does parity setting between the computer and the AJ71C24 match?
NO
Correct the parity setting.
YES
Does the data length setting between the computer and the AJ71C24 match?
NO
Correct the data length setting.
YES
Does the stop bit setting between the computer and the AJ71C24 match?
NO
Correct the stop bit setting.
YES
Do the computer and the AJ71C24 transmission speed settings match?
NO
Match the computer and the AJ71C24 transmission speed settings.
YES
Is the terminal resistance set to "present" at the end stations of the multidrop link?
NO
Set the terminal resistance to "present".
YES
Are all interfaces set to mode 1 to 8 to work independently?
NO
Set the modes correctly.
YES
Consult the nearest Mitsubishi representative.

* If mode 9 to D is set when interfaces are working independently, noise interference may occur between used and unused interfaces.

APPENDICES

APPENDIX 1. Precautions Concerning Compatibility and the Use of Existing Programs Prepared for the AJ71C24 Computer Link Module

The following sections describe precautions which should be taken when using the AJ71C24-S8 computer link module (hereafter called the AJ71C24-S8). These precautions cover compatibility with the AJ71C24 computer link module (hereafter called the AJ71C24), the use of existing programs prepared for the AJ71C24, and procedures for changing, adding, and installing modules to the existing network.

1.1 Compatibility

The AJ71C24-S8 and the AJ71C24 have the same dimensions and can be installed in the same way. They also use the same basic programs (PC CPU programs and computer programs).

Compatibility is maintained within the functions supported by the AJ71C24.

1.2 Precautions When Using Existing Programs

(1) Buffer memory read/write operations (CR and CW commands)

Addresses 100H to 11FH in the buffer memory of the AJ71C24-S8 are allocated for special applications.

Therefore, to read buffer memory or write data to the buffer memory using the CR or CW commands, use the memory areas in addresses 120H and above.

(2) Input/output for PC CPU

The READY signal Xn7 is provided for the AJ71C24-S8.

For the link operating in the no-protocol mode, this READY signal should be inserted (as the interlock signal) in the sequence program which uses the AJ71C24.

(3) Communications time

The time required for communications with a PC CPU differs between the AJ71C24 and the AJ71C24-S8. The User's Manual for each type of module gives details.

1.3 Function Comparison

Function \ Module					AJ71C24	AJ71C24-S8	See Section
Module READY signal					—	Xn7 of the I/O signals for the PC CPU is used as the READY signal.	3.4
RS-232C CD terminal check					Always checked.	Set whether or not the AJ71C24-S8 checks the CD signal.	3.2.2 7.1
Transmission error information			Display area		Error occurrence is confirmed by the LED on the front panel of the module.	Since the ON/OFF status of the error LED is stored in buffer memory, communications errors can be checked with the PC CPU by reading the buffer memory with a sequence program.	3.3.3
			To turn OFF the error display		The PC CPU must be reset.	The request signal to turn the error display OFF can be output with a sequence program.	
Dedicated protocols 1 to 4	—			Command	—	—	—
	Extension file registers	Batch read		ER	—	Extension file registers (R) are read in units of each register.	8.8
		Batch write		EW		Data is written to extension file registers (R) in units of each register.	
		Test (random write)		ET		To write data, block numbers and device numbers are designated for the extension file registers (R) at random in units of each register.	
		Monitor data registration		EM		The extension file registers (R) to be monitored are set in units of each register.	
		Monitor		ME		The extension file registers (R), set for monitoring, are monitored.	
	Microcomputer program	Batch read	Main	UR		Main microcomputer program is read.	8.12.5
			Sub	VR		Sub microcomputer program is read.	
		Batch write	Main	UW		Main microcomputer program is written.	
			Sub	VW		Sub microcomputer program is written.	8.12.6
	Comment	Batch read		KR		Comments are read from memory.	
		Batch write		KW		Comments are written to memory.	
	On-demand				Data transmission start is controlled by the computer.	The send request can be output from the PC CPU for data transmission with dedicated protocols 1 to 4.	8.14
	Communications with the PC CPU in MELSECNET(II) or MELSECNET/B				Communications is possible only with the PC CPU which is loaded with the AJ71C24.	Communications is possible with a PC CPU which is not loaded with the AJ71C24 in MELSECNET(II) or MELSECNET/B.	8.4.5 (4)
	Data communications using AnACPU dedicated commands with an A2ACPU(-S1) and A3ACPU.				—	Using AnACPU dedicated commands, data communications is possible with all device memories, extension file registers, and extension comments of an A2A/A3ACPU.	3.3.1 (2) 8

Function \ Module		AJ71C24	AJ71C24-S8	See Section
No-Protocol	Setting the receive completed code	Fixed at CR, LF (0DH, 0AH)	Setting is possible as required. (Default : CR, LF [0DH, 0AH])	7.4.1
	Setting the receive-completion data length (Data receive by fixed length)	Fixed at 127 words (254 bytes)	Setting is possible as required. (Default : 127 words)	7.4.2
	Send/receive data unit setting (word/byte)	Fixed at "words".	Setting is possible as required ("words" or "bytes"). (Default : Words)	7.4.3
	Setting the send buffer memory	Fixed as below: Head address 0H Buffer memory size 80H	Setting is possible as required excluding the memory area of 100H to 11FH. (Default : Head address 0H, Buffer memory size 80H)	7.4.4
	Setting receive buffer memory	Fixed as below: Head address 80H Buffer memory size 80H	Setting is possible as required excluding the memory area of 100H to 11FH. (Default : Head address 80H, Buffer memory size 80H)	7.4.5
	Receive data clear request	To clear the received data after an error occurs, the CPU must be reset. This means that the data received using the dedicated protocol is also cleared at the same time.	The data received in the no-protocol mode can only be cleared (without influencing the communications using the dedicated protocol) by using a sequence program.	9.5
Bidirectional	Data communications control with a computer (RS-232C or RS-422)	—	Data communications with a computer in the bidirectional mode is possible. (Possible in a 1-to-1 base system configuration)	7.5 10
Mode switching		—	The modes used with the RS-422 and RS-232C interfaces can be switched after the AJ71C24-S8 is started up. Dedicated protocol No-protocol ⟷ Bidirectional	3.4 7.6.2
Transmission control		●RS-232C interface Transmission is controlled by the DTR/DSR control. ●RS-422 interface Control is not available.	●RS-232C interface Transmission control by the DTR/DSR control or the DC code control is enabled. ●RS-422 interface Transmission control by the DC code control is enabled.	3.5 7.7
Data communications control in the half-duplex transmission (RS-232C)		—	Data communications with an external device supporting the half-duplex transmission function can be controlled according to the setting by the user.	5
"m : n" multidrop link			Data communications in the multidrop link in which the ratio of computers to PC CPUs is "m : n" is possible.	6

APPENDIX 2. Precautions Concerning Compatibility and the Use of Existing Programs Prepared for the AJ71C24-S3 Computer Link Module

The following sections describe precautions which should be taken when using the AJ71C24-S8 computer link module. These precautions cover compatibility with the AJ71C24-S3 computer link module (hereafter called the AJ71C24-S3), the use of existing programs prepared for the AJ71C24-S3, and procedures for changing, adding, and installing modules to the existing network.

2.1 Compatibility

The AJ71C24-S8 and the AJ71C24-S3 have the same dimensions and can be installed in the same way. They also use the same basic programs (PC CPU programs and computer programs).

Compatibility is maintained within the functions supported by the AJ71C24-S3.

2.2 Precautions When Using Existing Programs

(1) Communications time

The time required for communications with a PC CPU differs between the AJ71C2-S3 and the AJ71C24-S8. The User's Manual for each type of module gives details.

(2) PC CPU model name read function (command: PC)

When reading the PC model name of the PC CPU using the PC command, the model name codes for the A2ACPU(-S1), A3ACPU, etc. are changed.

CPU Model Name	AJ71C24-S3	AJ71C24-S8
A0J2HCPU	A2H	98H
A2ACPU	A4H	92H
A2ACPU-S1	A4H	93H
A3ACPU	A4H	94H
A1SCPU	A2H	98H
A2CCPU	A2H	9AH
A1SCPU	A2H	98H
A2CCPU	A2H	9AH

2.3 Function Comparison

Function \ Module		AJ71C24-S3	AJ71C24-S8	See Section
Dedicated protocols 1 to 4	Data communications using AnACPU dedicated commands with the A2ACPU(-S1) and A3ACPU.	—	Using the AnACPU dedicated commands, data communications is possible with all device memories, extension file registers, and extension comments of the A2A/A3ACPU.	3.3.1 (2) 8
Bidirectional	Data communications control with a computer (RS-232C or RS-422)		Data communications with a computer in the bidirectional mode is possible. (Possible in a 1-to-1 base system configuration)	7.5 10
Mode switching		—	The modes used with the RS-422 and RS-232C interfaces can be switched after the AJ71C24-S8 is started up. Dedicated protocol No-protocol ⟷ Bidirectional	3.4 7.6.2
Transmission control		●RS-232C interface Transmission is controlled by the DTR/DSR control. ●RS-422 interface Control is not available.	●RS-232C interface Transmission control by the DTR/DSR control or the DC code control is enabled. ●RS-422 interface Transmission control by the DC code control is enabled.	3.5 7.7
Data communications control in the half-duplex transmission (RS-232C)		—	Data communications with an external device supporting the half-duplex transmission function can be controlled according to the setting by the user.	5
"m : n" multidrop link			Data communications in the multidrop link in which the ratio of computers to PC CPUs is "m : n" is possible.	6

APPENDIX 3. Precautions Concerning Compatibility and the Use of Existing Programs Prepared for the AJ71C24-S6 Computer Link Module

The following sections describe precautions which should be taken when using the AJ71C24-S8 computer link module.

These precautions cover compatibility with the AJ71C24-S6 computer link module (hereafter called the AJ71C24-S6), the use of existing programs prepared for the AJ71C24-S6, and procedure for changing or adding modules in the existing network.

3.1 Compatibility

The AJ71C24-S8 and the AJ71C24-S6 have the same dimensions and can be installed in the same way. They also use the same basic programs (on a PC CPU and a computer).

Compatibility is maintained within the functions supported by the AJ71C24-S6.

3.2 Precautions When Using Existing Programs

None when the AJ71C24-S6 is replaced by an AJ71C24-S8.

3.3 Function Comparison

The following table compares the functions of the AJ71C24-S6 and AJ71C24-S8.

Function \ Module	AJ71C24-S6	AJ71C24-S8	See Section
Mode switching	—	The modes used with the RS-422 and RS-232C interfaces can be switched after the AJ71C24-S8 is started up. Dedicated protocol No-protocol ⟷ Bidirectional	3.4 7.6.2
Transmission control	●RS-232C interface Transmission is controlled by the DTR/DSR control. ●RS-422 interface Control is not available.	●RS-232C interface Transmission control by the DTR/DSR control or the DC code control is enabled. ●RS-422 interface Transmission control by the DC code control is enabled.	3.5 7.7

APPENDIX 4. ASCII Code Table

Character codes used for the computer link are shown below. (7-bit codes)

LSD \ MSD		0	1	2	3	4	5	6	7
LSD		000	001	010	011	100	101	110	111
0	0000	NUL	DLE	SP	0	@	P	`	p
1	0001	SOH	DC1	!	1	A	Q	a	q
2	0010	STX	DC2	"	2	B	R	b	r
3	0011	ETX	DC3	#	3	C	S	c	s
4	0100	EOT	DC4	$	4	D	T	d	t
5	0101	ENQ	NAK	%	5	E	U	e	u
6	0110	ACK	SYN	&	6	F	V	f	v
7	0111	BEL	ETB	'	7	G	W	g	w
8	1000	BS	CAN	(	8	H	X	h	x
9	1001	HT	EM	)	9	I	Y	i	y
A	1010	LF	SUB	*	:	J	Z	j	z
B	1011	VT	ESC	+	;	K	[	k	{
C	1100	FF	FS	,	<	L	\	l	|
D	1101	CR	GS	-	=	M	]	m	}
E	1110	SO	RS	.	>	N	↑	n	~
F	1111	SI	VS	/	?	O	←	o	DEL

APPENDIX 5. Communications Time between a PC CPU and an AJ71C24

When the PC CPU is in the run state, data is processed after executing the END instruction in response to a request from the AJ71C24. Section 3.3.1 gives the minimum number of devices processed per communications.

The intervening times (i.e. by how much the scan time increases) for each processing operation and its corresponding processing times (indicated in number of scans) are shown below.

(1) ACPU common command

Item				Command	Intervening Times (Scan Time Increases)				Scan Count Required for Processing
					A0J2H, A1N, A2N, A3N	A3H	A2A, A3A	Access Data Unit	
Device data	Device memory	Batch read	Bit units	BR	0.76 ms	0.57 ms	1.38 ms	256 devices	1 scan (2 scans for device "R" only)
			Word devices	WR	1.13 ms	0.81 ms	2.42 ms	64 devices	
		Batch write	Bit units	BW	1.13 ms	0.94 ms	1.06 ms	160 devices	2 scans (1 scan when "enable during RUN" is set [excluding R])
			Word devices	WW	1.13 ms	0.84 ms	2.60 ms	64 devices	
		Test (random write)	Bit units	BT	1.13 ms	0.90 ms	1.06 ms	20 devices	2 scans (1 scan when "enable during RUN" is set [excluding R])
			Word devices	WT	1.13 ms	0.90 ms	1.06 ms	10 devices	
		Monitor data registration	Bit units	BM	—	—	—	—	—
			Word devices	WM					1 scan for device "R" only
		Monitor	Bit units	MB	2.02 ms	0.93 ms	1.46 ms	40 devices	1 scan
			Word devices	MN	2.08 ms	0.96 ms	1.47 ms	20 devices	
	Extension file register	Batch read		ER	1.27 ms	0.76 ms	2.42 ms	64 devices	2 scan (3 scans for ET [only AnACPU])
		Batch write		EW	1.27 ms	0.76 ms	2.60 ms	64 devices	
		Test (Random write)		ET	1.31 ms	0.87 ms	0.97 ms	10 devices	
		Monitor data registration		EM	—	—	—	—	—
		Monitor		ME	1.75 ms	0.98 ms	1.42 ms	20 devices	1 scan
	Buffer memory	Batch read		CR	—	—	—	—	—
		Batch write		CW					

Item				Command	Intervening Times (Scan Time Increases)				Scan Count Required for Processing
					A0J2H, A1N, A2N, A3N	A3H	A2A, A3A	Access Data Unit	
Special function module buffer memory		Batch read		TR	FROM instruction processing time + 1.13 msec	FROM instruction processing time + 0.81 msec	FROM instruction processing time + 0.75 msec	128 bytes	1 scan
		Batch write		TW					2 scans (1 scan when "enable during RUN" is set)
Program	Sequence program	Batch read	Main	MR	1.20 ms	0.78 ms	0.70 ms	64 steps	1 scan
			Sub	SR	1.20 ms	0.84 ms	0.70 ms		
		Batch write	Main	MW	0.67 ms	0.55 ms	0.49 ms		2 scans (1 scan when "enable during RUN" is set)
			Sub	SW	0.67 ms	0.55 ms	0.49 ms		
	Microcomputer program	Batch read	Main	UR	1.35 ms	0.76 ms	—	128 bytes	2 scans
			Sub	VR	1.35 ms	0.76 ms			
		Batch write	Main	UW	1.35 ms	0.76 ms			
			Sub	VW	1.53 ms	0.73 ms			
	Comment	Batch read		KR	1.35 ms	0.76 ms	2.42 ms	128 bytes	2 scans
		Batch write		KW	1.53 ms	0.73 ms	2.60 ms		
	Parameter	Batch read		PR	0.68 ms	0.50 ms	2.42 ms	128 bytes	2 scans
		Batch write		PW	—	—	—	—	—
		Analysis request		PS					
PC CPU		Remote RUN		RR	—	—	—	—	—
		Remote STOP		RS					
		PC type read		PC	—	—	—	—	—
Global				GW	—	—	—	—	—

(2) AnACPU dedicated command

Item				Com-mand	Intervening Times (Scan Time Increases)		Scan Count Required for Processing
					A2A, A3A	Access Data Unit	
Device data	Device memory	Batch read	Bit units	JR	1.19 ms	256 devices	1 scan (2 scans for device "R" only)
			Word units	QR	2.07 ms	64 devices	
		Batch write	Bit units	JW	0.99 ms	160 devices	2 scans (1 scan when "enable during RUN" is set [excluding R])
			Word units	QW	2.32 ms	64 devices	
		Test (random write)	Bit units	JT	0.91 ms	20 devices	2 scans (1 scan when "enable during RUN" is set [excluding R])
			Word units	QT	0.93 ms	10 devices	
		Monitor data registration	Bit units	JM	—	—	—
			Word units	QM			1 scan for device "R" only
		Monitor	Bit units	MJ	1.34 ms	40 devices	1 scan
			Word units	MQ	1.35 ms	20 devices	
	Extension file register	Direct read		NR	2.30 ms	64 devices	3 scans (4 scans when a set range covers several blocks)
		Direct write		NW	2.57 ms	64 devices	
Program	Extension comment	Batch read		DR	2.31 ms	128 bytes	2 scans
		Batch write		DW	2.59 ms		

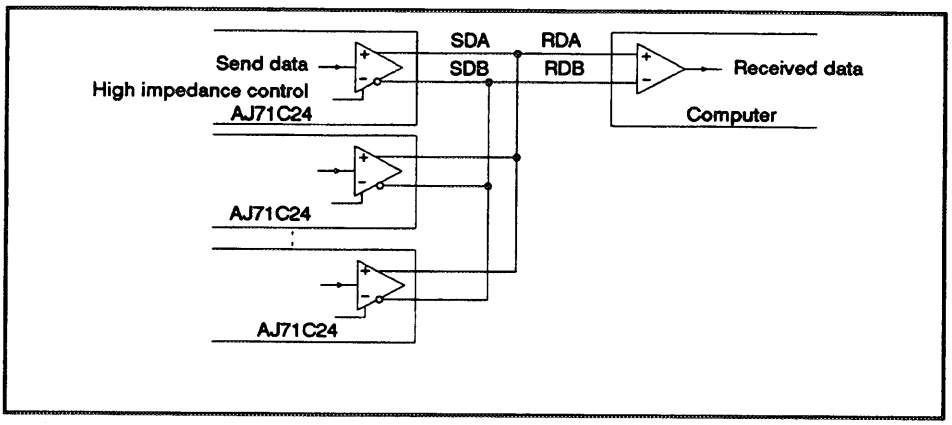
POINTS

(1) The PC CPU can only process one of these operations with each END processing. If the A6GPP and AJ71C24 access a given PC CPU at the same time, one processing must wait until the other processing is completed. Therefore, the scan count required for processing further increases.

(2) Even though communications using AJ71C24 is not performed, scan time increases 0.2 msec (0.1 msec with A3HCPU, A2ACPU(S1), and A3ACPU).

APPENDIX 6. Precautions During Communications When Using RS-422 Interface

(1) The following figure shows the hardware structure for the data transmission from the AJ71C24 to the computer.



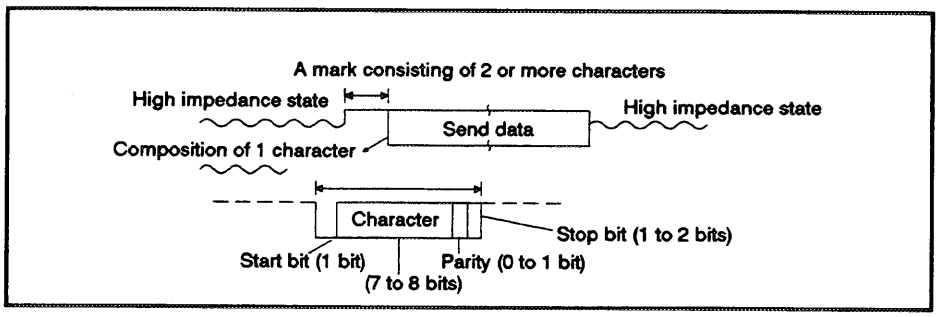
AJ71C24 Send Circuit

(2) Data transmission methods

When each station of the AJ71C24 is not transmitting data, set the transmission line to the high impedance state so that one send data does not interfere with other send data in a multidrop link.

When all stations transmit data, the high impedance state must be canceled. Then, after transmitting a mark consisting of 2 or more characters, each station transmits data.

This method applies also to a 1:1 link system.


A mark consisting of 2 or more characters
High impedance state
High impedance state
Send data
Composition of 1 character
Character
Stop bit (1 to 2 bits)
Start bit (1 bit)
Parity (0 to 1 bit)
(7 to 8 bits)

Transmission from the AJ71C24

(3) Ignoring wrong data

When any station is not transmitting data, the send line is in the high impedance state.

Thus, the send line may become unstable due to noise, causing a computer to receive wrong data.

Since a parity error or a framing error may occur in this case, error data must be ignored.

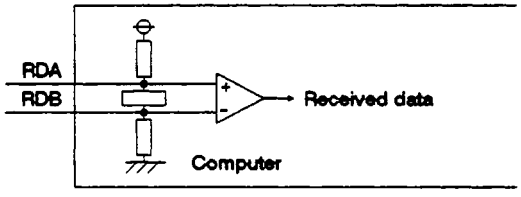
When using protocol 1 to 4, either ACK, NAK, or STX code is transmitted first.

Therefore until an ACK, NAK, or STX code is received, other codes must be ignored.

POINT

When a computer has a pull-up/down register, wrong data is not received.

When a computer does not have a pull-up/down register, insert a resistance (4.7 KΩ 1/4W as a standard resistance value) to prevent a receive of wrong data.



APPENDIX 7. Special Function Module Buffer Memory Addresses

The special function module buffer memory addresses are listed below. They are used to read and write (commands TR, TW) data to and from the special function module buffer memory with protocols 1 to 4.

The appropriate manuals give details about buffer memory contents.

(1) Linkable special function modules, buffer memory head address, and module numbers

Special Function Module Name	Buffer Memory Head Address (hexadecimal)	Module Number When Loaded in Slot No. 0
AD61(S1) high-speed counter module	80H	01H
A616AD analog-digital converter module	10H	01H
A616DAI digital-analog converter module	10H	01H
A616DAV digital-analog converter module	10H	01H
A616TD temperature-digital converter module	10H	01H
A62DA(S1) digital-analog converter module	10H	01H
A68AD(S2) analog-digital converter module	80H	01H
A68ADN analog-digital converter module	80H	01H
A84AD analog-digital converter module	10H	02H
A81CPU PID control module	200H	03H
A61LS position detection module	80H	01H
A62LS position detection module	80H	02H
AD70(D) positioning module	80H	01H
AD71(S1) positioning module	200H	01H
AD71-S2 positioning module	200H	01H
AD72 positioning module	200H	02H
AJ71PT32 MELSECNET/MINI master module	20H	01H
AJ71C22 multidrop link module	1000H	01H
AJ71C24(S3/S6) computer link module	1000H	01H
AD51(S3) intelligent communications module	800H	02H
AD51H intelligent communications module	800H	02H
AD57G graphic controller module	280H	02H
AJ71C21(S1) terminal interface module	400H	01H
AJ71B62 B/NET interface module	20H	01H
AJ71P41 SUMINET interface module	400H	01H
AJ71E71 Ethernet interface module	400H	01H
A1SD61 high-speed counter module	80H	01H
A1S62DA digital-analog converter module	10H	01H
A1S62RD3/4 temperature-digital converter module	10H	01H
A1S64AD analog-digital converter module	80H	01H
A1SJ71C24 -R2 computer link module	400H	01H

(2) Buffer memory address tables of special-function modules

This section gives the address tables of the following special-function modules:

- AJ71C24(-S3,-S6,-S8) computer link module
- AD61 high-speed counter module
- AD71(S1) and AD71-S2 positioning module
- A616DAI(DAV) digital-analog converter module

Calculate the addresses of special-function modules not mentioned above by using the following formula and the head addresses given in (a) on the next page.

- Formula

The following formula converts the address (hexadecimal) to be designated in a computer using the address for the FROM/TO instructions.

Designated address (hexadecimal) =
Address used with FROM/TO instructions x 2 converted into hexadecimal + Head address of each module

The User's Manual for each module gives details about the addresses of FROM/TO instructions.

Calculation example 1:

To designate the head address (the designated address of the FROM/TO instructions is 100H) of the special-applications area of the AJ71C24-S8

Designated address (1200H) =

Address used with FROM/TO instructions (100H) x 2 (200H)
+ Head address (1000H)

Calculation example 2:

To designate the preset value storage address (the designated address of the FROM/TO instructions is 1H) of CH1 of the AD61 high-speed counter module

Designated address (82H) =

Address used with FROM/TO instructions (1H) x 2 (2H)
+ Head address (80H)

(a) AJ71C24 (-S3,-S6,-S8) computer link module

Buffer Memory Contents	Address Set by Computer	Address Set with FROM/TO Instructions
User area	1000H to 11FFH	0 to FFH
Special applications area (except for the AJ71C24 computer link module)	1200H to 123FH	100H to 11FH
User area	1240H to 1FFFH	120H to 7FFH

(See Section 3.7.)

REMARK

Addresses 1000H to 1FFFH of the AJ71C24 (set by a computer) are the buffer memory addresses utilized when using a computer to execute read/write from/to an AJ71C24 not connected to a computer.

(b) AD61(S1) high-speed counter module

Buffer Memory Contents	Address Set by Computer		Address Set with FROM/TO Instruction	
	Channel 1	Channel 2	CH1	CH2
Unused area (unavailable)	80H	C0H	0	32
	81H	C1H		
Current value write (lower bits)	82H	C2H	1	33
Current value write (middle bits)	83H	C3H		
Current value write (higher bits)	84H	C4H	2	34
	85H	C5H		
Mode register	86H	C6H	3	35
	87H	C7H		
Current value read (lower bits)	88H	C8H	4	36
Current value read (middle bits)	89H	C9H		
Current value read (higher bits)	8AH	CAH	5	37
	8BH	CBH		
Set value read/write (lower bits)	8CH	CCH	6	38
Set value read/write (middle bits)	8DH	CDH		
Set value read/write (higher bits)	8EH	CEH	7	39
	8FH	CFH		

(c) AD71(S1) and AD71-S2 positioning modules

Buffer Memory Contents		Address Set by Computer	Address Set with FROM/TO Instruction
X-axis positioning start data		200H to 391H	0 to 200
Error reset		392H 393H	201
Y-axis positioning start data		458H to 5E9H	300 to 500
Positioning information	X-axis positioning data	2040H to 235FH	3872 to 4271
Positioning velocity		2360H to 267FH	4272 to 4671
Dwell time		2680H to 299FH	4672 to 5071
Positioning address		29A0H to 2FDFH	5072 to 5871
Positioning information	Y-axis positioning data	2FE0H to 32FFH	5872 to 6271
Positioning velocity		3300H to 361FH	6272 to 6671
Dwell time		3620H to 393FH	6672 to 7071
Positioning address		3640H to 3F7FH	7072 to 7871
X-axis parameter		3F80H to 3F9FH	7872 to 7887
Y-axis parameter		3FA8H to 3FC7H	7892 to 7907
X-axis zero return data		3FD0H to 3FDDH	7912 to 7917
Y-axis zero return data		3FE4H to 3FF1H	7922 to 7928

(d) A616DAI digital-analog converter module

A616DAI digital-analog converter module

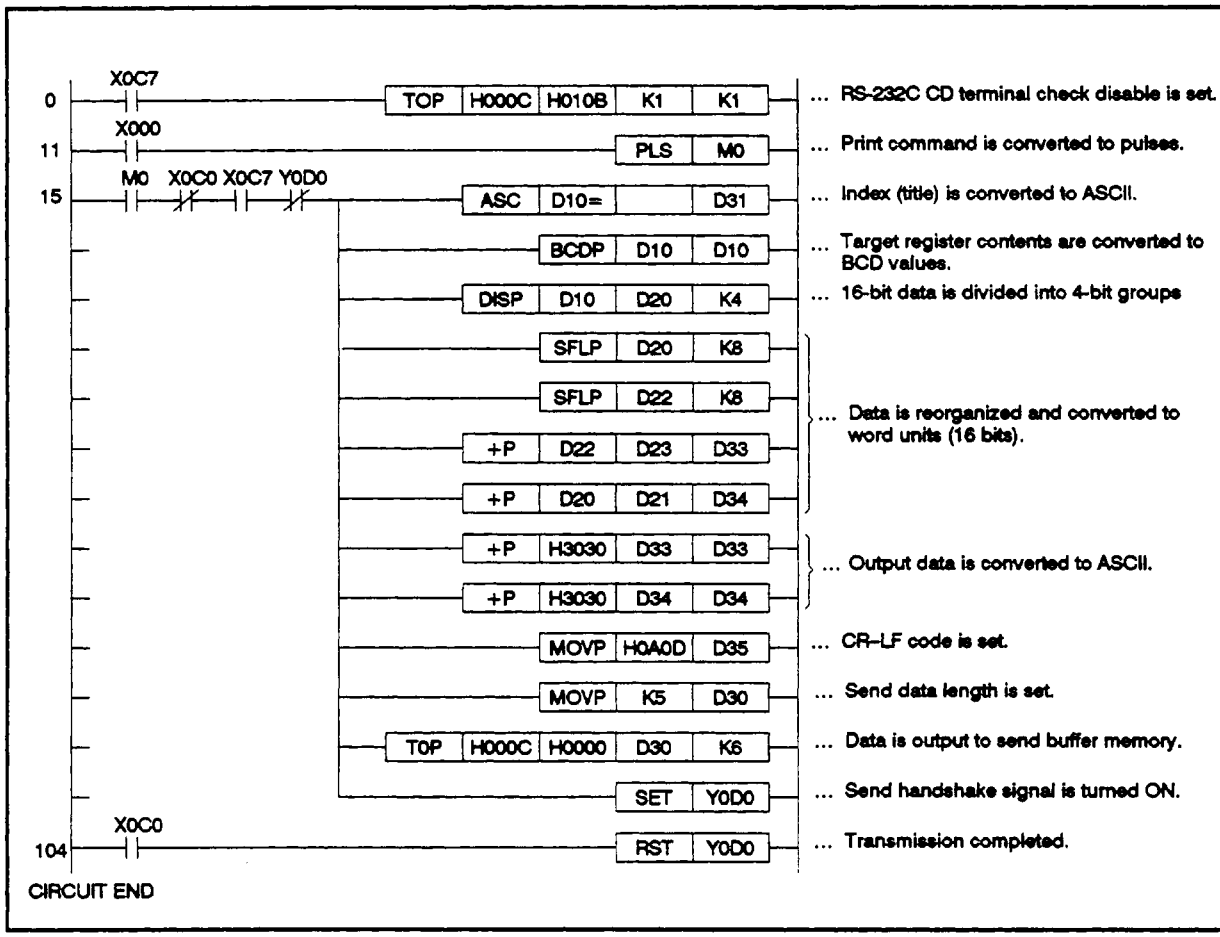
Buffer Memory Contents	Address Set by Computer	Address Set with FROM/TO Instruction
D-A conversion enable/disable channel	10H	0H
Analog output enable/disable channel	12H	1H
Unused area (unavailable)	—	2H to FH
CH. 0 digital value	30H	10H
CH. 1 digital value	32H	11H
CH. 2 digital value	34H	12H
CH. 3 digital value	36H	13H
CH. 4 digital value	38H	14H
CH. 5 digital value	3AH	15H
CH. 6 digital value	3CH	16H
CH. 7 digital value	3EH	17H
CH. 8 digital value	40H	18H
CH. 9 digital value	42H	19H
CH. A digital value	44H	1AH
CH. B digital value	46H	1BH
CH. C digital value	48H	1CH
CH. D digital value	4AH	1DH
CH. E digital value	4CH	1EH
CH. F digital value	4EH	1FH
Unsed area (unavailable)	—	20H to 2FH
CH. 0 set value check code	70H	30H
CH. 1 set value check code	72H	31H
CH. 2 set value check code	74H	32H
CH. 3 set value check code	76H	33H
CH. 4 set value check code	78H	34H
CH. 5 set value check code	7AH	35H
CH. 6 set value check code	7CH	36H
CH. 7 set value check code	7EH	37H
CH. 8 set value check code	80H	38H
CH. 9 set value check code	82H	39H
CH. A set value check code	84H	3AH
CH. B set value check code	86H	3BH
CH. C set value check code	88H	3CH
CH. D set value check code	8AH	3DH
CH. E set value check code	8CH	3EH
CH. F set value check code	8EH	3FH

APPENDIX 8. Sequence Program Examples Showing How to Output Word Device Data to the Printer in the No-protocol Mode

This program gives an example of outputting the data registers (D), link registers (W) and file registers (R), and present values of timers and counters to the printer in the no-protocol mode.

8.1 When Other Than AnACPU is Used

(1) Sequence program example


X0C7
0
TOP H000C H010B K1 K1 ... RS-232C CD terminal check disable is set.
X000
11
PLS M0 ... Print command is converted to pulses.
M0 X0C0 X0C7 Y0D0
15
ASC D10= D31 ... Index (title) is converted to ASCII.
BCDP D10 D10 ... Target register contents are converted to BCD values.
DISP D10 D20 K4 ... 16-bit data is divided into 4-bit groups
SFLP D20 K8
SFLP D22 K8
+P D22 D23 D33
+P D20 D21 D34
... Data is reorganized and converted to word units (16 bits).
+P H3030 D33 D33
+P H3030 D34 D34
... Output data is converted to ASCII.
MOVP H0A0D D35 ... CR-LF code is set.
MOVP K5 D30 ... Send data length is set.
TOP H000C H0000 D30 K6 ... Data is output to send buffer memory.
SET Y0D0 ... Send handshake signal is turned ON.
X0C0
104
RST Y0D0 ... Transmission completed.
CIRCUIT END

REMARK

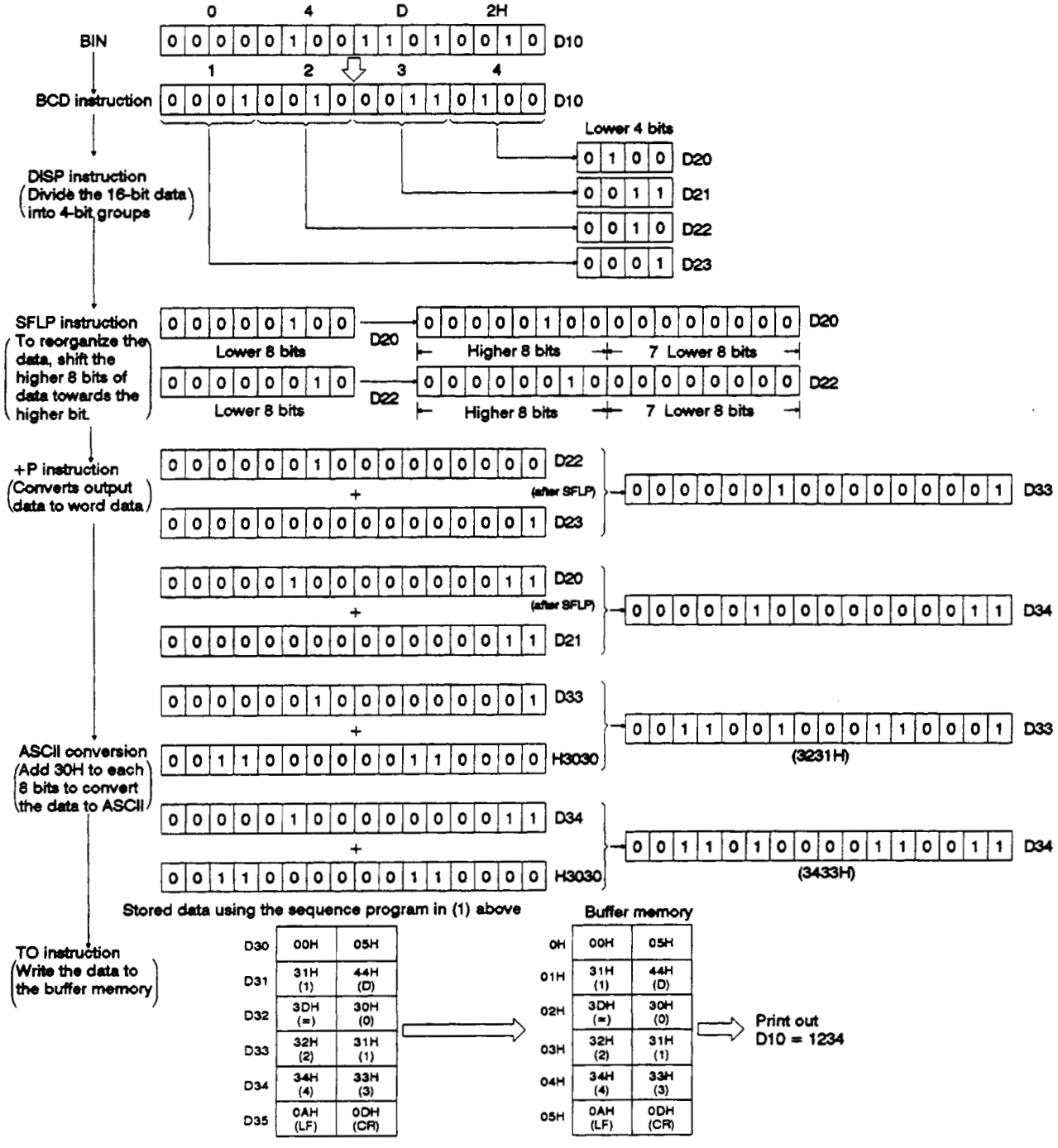
AJ71C24 transmission specification settings for output to printer

	K6PR	K6PR-K	K7PR	A7PR
Baud rate	2400	2400	9600	9600
Data length	8	8	8	8
Stop bits	1	1	2	1
Parity check	Even	Even	None	Even
Comments			Baud rate can be changed to 2400	

(2) Procedure for converting data stored in a data register to printer output data.

Since the PC CPU handles numerical data in binary, it is necessary to convert data to be printed out from binary (BIN) to ASCII. Data is output from the buffer memory to the printer sequentially from the lowest address (head address) with the lower 8 bits to the higher 8 bits. Therefore, use the sequence program to reorganize the order of the data output to the printer. The following program, described in (1), gives an example of this conversion.

Example: Converting "1234" stored in the data register to ASCII

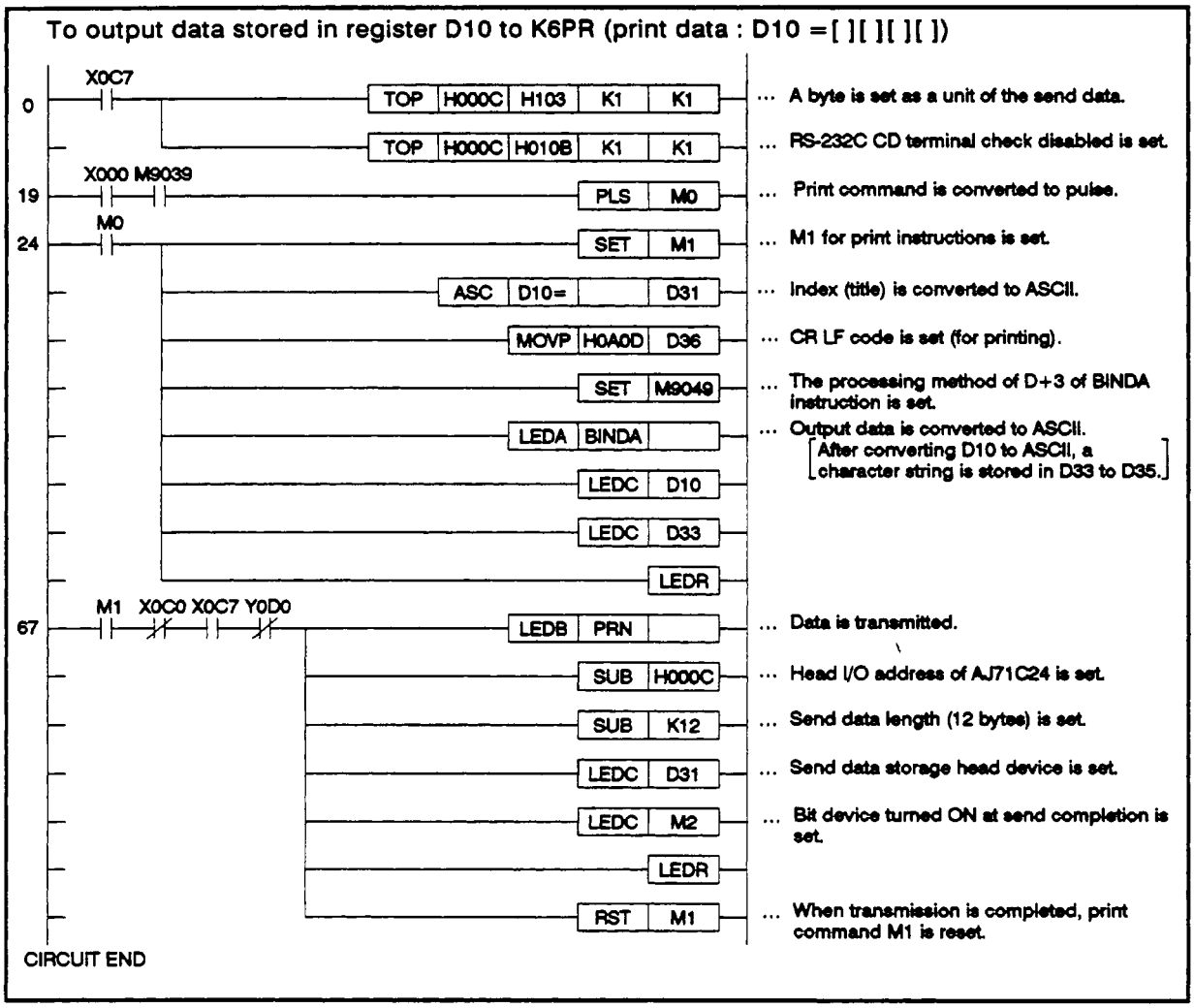


D30	00H	05H
D31	31H (1)	44H (D)
D32	3DH (=)	30H (0)
D33	32H (2)	31H (1)
D34	34H (4)	33H (3)
D35	0AH (LF)	0DH (CR)

0H	00H	05H
01H	31H (1)	44H (D)
02H	3DH (=)	30H (0)
03H	32H (2)	31H (1)
04H	34H (4)	33H (3)
05H	0AH (LF)	0DH (CR)

8.2 When the AnACPU is Used

The following is a program example using A2A(-S1)/A3ACPU dedicated instruction (BINDA) to execute the same processing as the program shown in 8.1.

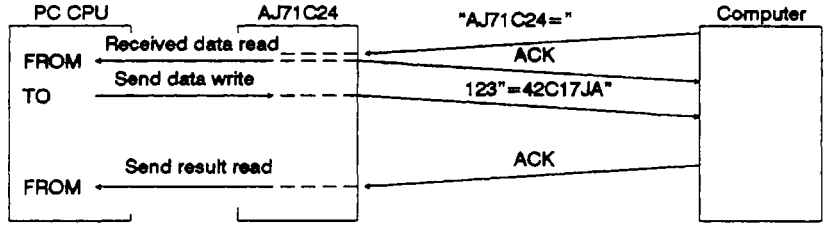

To output data stored in register D10 to K6PR (print data : D10 =[ ][ ][ ][ ])
X0C7
0
TOP H000C H103 K1 K1
... A byte is set as a unit of the send data.
TOP H000C H010B K1 K1
... RS-232C CD terminal check disabled is set.
X000 M9039
19
PLS M0
... Print command is converted to pulse.
M0
24
SET M1
... M1 for print instructions is set.
ASC D10= D31
... Index (title) is converted to ASCII.
MOVP H0A0D D36
... CR LF code is set (for printing).
SET M9049
... The processing method of D+3 of BINDA instruction is set.
LEDA BINDA
... Output data is converted to ASCII.
After converting D10 to ASCII, a character string is stored in D33 to D35.
LEDC D10
LEDC D33
LEDR
M1 X0C0 X0C7 Y0D0
67
LEDB PRN
... Data is transmitted.
SUB H000C
... Head I/O address of AJ71C24 is set.
SUB K12
... Send data length (12 bytes) is set.
LEDC D31
... Send data storage head device is set.
LEDC M2
... Bit device turned ON at send completion is set.
LEDR
RST M1
... When transmission is completed, print command M1 is reset.
CIRCUIT END

REMARK

Appendix 8.1 gives the AJ71C24 transmission specification setting for outputting data to the printer.

APPENDIX 9. Example of a Sequence Program for Data Communications in the Bidirectional Mode

The following figure gives the example of a sequence program for transmitting data received from the computer and the data of the data register (D100) of a PC CPU to the computer in the bidirectional mode.



(1) Settings to the buffer memory

The figure below describes settings at the special-applications area of AJ71C24 buffer memory.

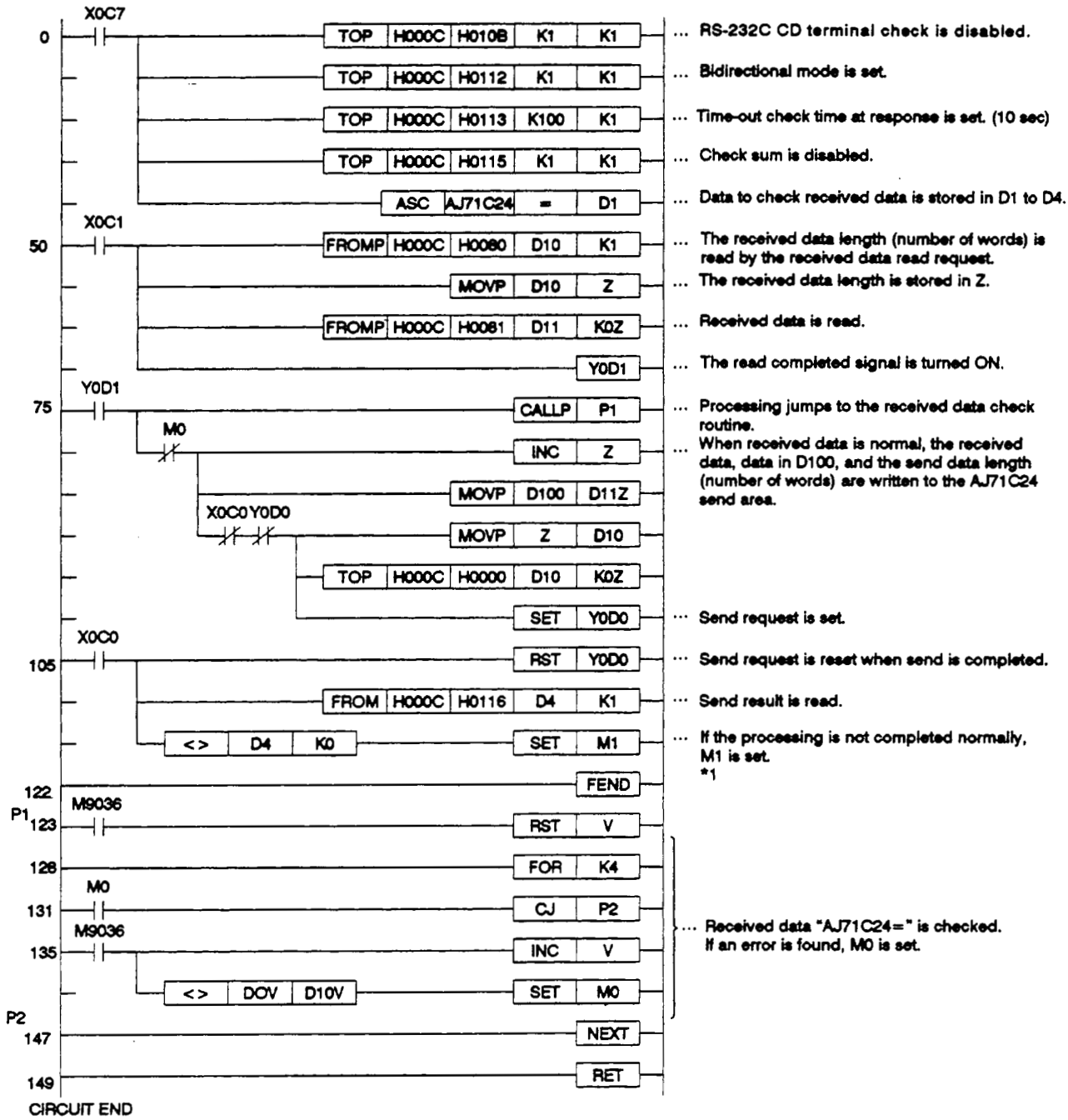
Appendix 11 gives details of the memory setting record form.

Buffer memory

Address	Dedicated Protocol	No-protocol	Bidirectional	Name	Set Value	Default Setting
100H	—	o	—	No-protocol receive-completed code setting area		0D0AH (CR, LF)
101H	—	—	—	Error LED ON status storage area	—	0
102H	—	—	—	Error LED turn OFF request area	—	0
103H	o	o	o	No-protocol word byte setting area		0 (words)
104H	—	o	o	No-protocol send buffer memory head address setting area		0
105H	—	o	o	No-protocol send buffer memory length setting area		80H
106H	—	o	o	No-protocol receive buffer memory head address setting area		80H
107H	—	o	o	No-protocol receive buffer memory length setting area		80H
108H	—	o	—	No-protocol receive-completion data length setting area		127 (words)
109H	—	—	—	On-demand buffer memory head address setting area	—	0
10AH	—	—	—	On-demand data length setting area	—	0
10BH	o	o	o	RS-232C CD terminal check setting area	1	0 (check CD enabled)
10CH	—	—	—	On-demand error storage area	—	0
10DH	—	—	—	No-protocol received data clear request area	—	0
10EH	—	—	—	System area (unavailable)	—	—
10FH	o	o	o	RS-232C communications mode setting area		0 (Full-duplex)
110H	o	o	o	Simultaneous transmission priority/non-priority setting area		0 (Priority)
111H	o	o	o	Transmission method at transmission resume		0 (Not retransmitted)
112H	—	—	o	Bidirectional mode setting area	1	0 (No-protocol mode)
113H	—	—	o	Time-out check time setting area	100	0 (Infinite)
114H	—	—	o	Simultaneous transmission data valid/invalid setting area		0 (Data valid)
115H	—	—	o	Check sum enable/disable setting area	1	0 (Check sum enabled)
116H	—	—	—	Data send error storage area	—	—
117H	—	—	—	Data receive error storage area	—	—

Switch settings

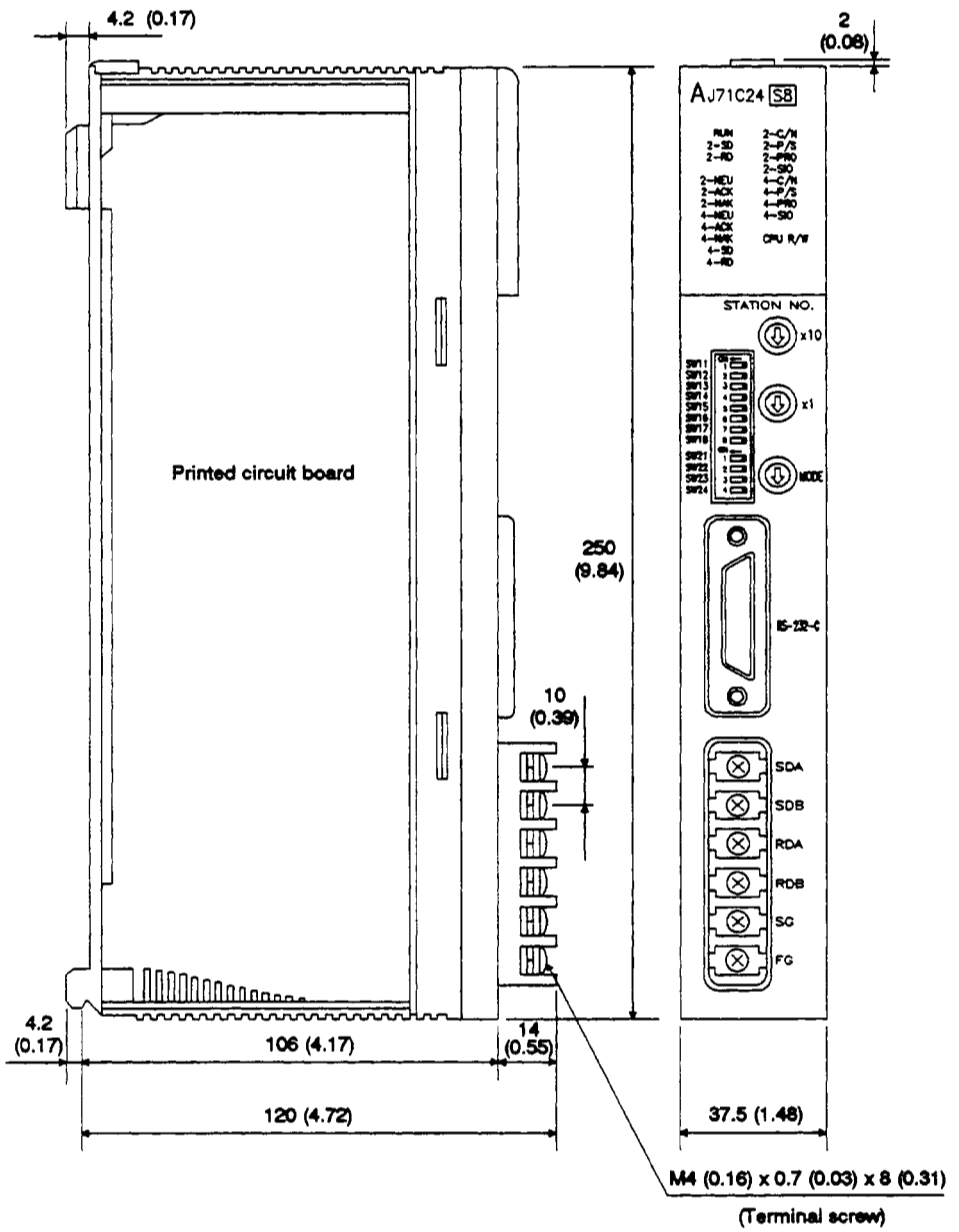
(2) Sequence program example


X0C7
0
TOP H000C H010B K1 K1 ... RS-232C CD terminal check is disabled.
TOP H000C H0112 K1 K1 ... Bidirectional mode is set.
TOP H000C H0113 K100 K1 ... Time-out check time at response is set. (10 sec)
TOP H000C H0115 K1 K1 ... Check sum is disabled.
ASC AJ71C24 = D1 ... Data to check received data is stored in D1 to D4.
X0C1
50
FROMP H000C H0080 D10 K1 ... The received data length (number of words) is read by the received data read request.
MOVP D10 Z ... The received data length is stored in Z.
FROMP H000C H0081 D11 K0Z ... Received data is read.
Y0D1 ... The read completed signal is turned ON.
Y0D1
75
CALLP P1 ... Processing jumps to the received data check routine.
M0
INC Z ... When received data is normal, the received data, data in D100, and the send data length (number of words) are written to the AJ71C24 send area.
MOVP D100 D11Z
X0C0 Y0D0
MOVP Z D10
TOP H000C H0000 D10 K0Z
SET Y0D0 ... Send request is set.
X0C0
105
RST Y0D0 ... Send request is reset when send is completed.
FROM H000C H0116 D4 K1 ... Send result is read.
<> D4 K0
SET M1 ... If the processing is not completed normally, M1 is set. *1
122
FEND
P1
M9036
123
RST V
128
FOR K4
M0
131
CJ P2
M9036
135
INC V
... Received data "AJ71C24=" is checked. If an error is found, M0 is set.
<> DOV D10V
SET M0
P2
147
NEXT
149
RET
CIRCUIT END

*1 When an error occurs in the data send result

Perform error correction according to the error code read from buffer memory address 116H.

APPENDIX 10. External View



Unit: mm (inch)

APPENDIX 11. AJ71C24 Setting Record Form

Use this form to keep record of settings of the AJ71C24 or to create computer link programs for PC CPUs and computers.

Make duplications of this form and use them.

Method of entry

(1) No. and Data

Enter the number of the record form and the date on the top right corner of the form.

(2) Settings of the buffer memory special applications area

Enter the set values which change default settings when the AJ71C24 READY signal (Xn7) is turned ON in the set value's column.

The settings required for the dedicated protocol and the no-protocol/bidirectional mode at the start of the AJ71C24 are indicated with [ ] mark in the columns next to the address's column.

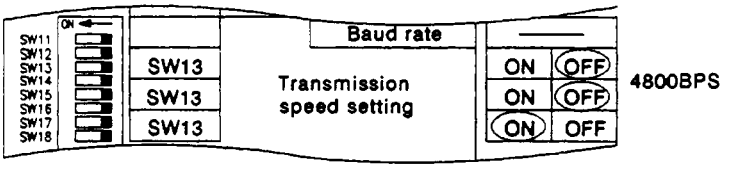
(3) Switch settings

1) Station number setting switch

Enter set values (value indicated by the arrow) in the columns of the tens digit and the ones digit of each station number.

2) Transmission specification switch settings

Circle ON or OFF according to switch setting from SW11 to SW24 in the ON/OFF column.



3) Mode switch settings

Enter the set value (value indicated by the arrow) in the mode setting switch column.

Record form No. Date : :

Record of AJ71C24 settings

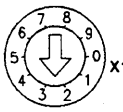
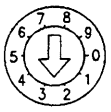
Settings of the buffer memory special applications area | Sections 3.5 and 7 of this manual give details.

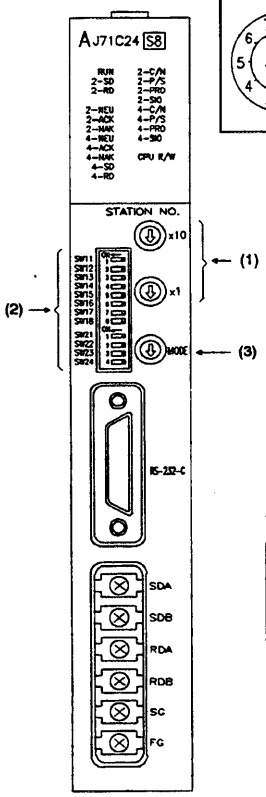
Buffer memory

Address	Dedicated Protocol	No-protocol	Bidirectional	Name	Set Value	Default Setting
100H	–	o	–	No-protocol receive-completed code setting area		0D0AH (CR, LF)
101H	–	–	–	Error LED ON status storage area	–	0
102H	–	–	–	Error LED turn OFF request area	–	0
103H	o	o	o	No-protocol word byte setting area		0 (words)
104H	–	o	o	No-protocol send buffer memory head address setting area		0
105H	–	o	o	No-protocol send buffer memory length setting area		80H
106H	–	o	o	No-protocol receive buffer memory head address setting area		80H
107H	–	o	o	No-protocol receive buffer memory length setting area		80H
108H	–	o	–	No-protocol receive-completion data length setting area		127 (words)
109H	–	–	–	On-demand buffer memory head address setting area	–	0
10AH	–	–	–	On-demand data length setting area	–	0
10BH	o	o	o	RS-232C CD terminal check setting area	1	0 (check CD enabled)
10CH	–	–	–	On-demand error storage area	–	0
10DH	–	–	–	No-protocol received data clear request area	–	0
10EH	–	–	–	System area (unavailable)	–	–
10FH	o	o	o	RS-232C communications mode setting area		0 (Full-duplex)
110H	o	o	o	Simultaneous transmission priority/non-priority setting area		0 (Priority)
111H	o	o	o	Transmission method at transmission resume		0 (Not retransmitted)
112H	–	–	o	Bidirectional mode setting area	1	0 (No-protocol mode)
113H	–	–	o	Time-out check time setting area	100	0 (Infinite)
114H	–	–	o	Simultaneous transmission data valid/invalid setting area		0 (Data valid)
115H	–	–	o	Check sum enable/disable setting area	1	0 (Check sum enabled)
116H	–	–	–	Data send error storage area	–	–
117H	–	–	–	Data receive error storage area	–	–
118H	–	–	–	Mode setting status storage area		1H to DH
119H	–	–	–	Mode switching setting area		0
11AH	o	o	o	Transmission time setting area		0 (DTR control)
11BH	o	o	o	DC1/DC3 control code setting area		1311H
11CH	o	o	o	DC2/DC4 control code setting area		1412H

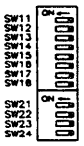
Set value of switch

1) Station number setting (See Section 4.3.3)

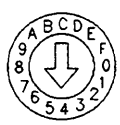
	Setting Contents	Set Value
	Tens digit of station number	
	Ones digit of station number	



2) Transmission specification setting switch (see Section 4.3.2.).

	Setting Switch	Setting Item	Set Value
	SW11	Main channel	ON OFF
	SW12	Data length	ON OFF
		Baud rate	–
	SW13	Transmission speed	ON OFF
	SW14		ON OFF
	SW15		ON OFF
	SW16	Parity bit	ON OFF
	SW17	Odd/even parity setting	ON OFF
	SW18	Stop bit	ON OFF
	SW21	Sum check	ON OFF
	SW22	Write during RUN	ON OFF
	SW23	Send side terminal resistance	ON OFF
	SW24	Receive side terminal resistance	ON OFF

3) Mode setting switch (see Section 4.3.1.).

	Mode Setting Switch No.	Setting		Set Value
		RS-232C	RS-422	
 MODE	0	Unavailable		
	1	Protocol 1 mode	No-protocol mode	
	2	Protocol 2 mode	No-protocol mode	
	3	Protocol 3 mode	No-protocol mode	
	4	Protocol 4 mode	No-protocol mode	
	5	No-protocol mode	Protocol 1 mode	
	6	No-protocol mode	Protocol 2 mode	
	7	No-protocol mode	Protocol 3 mode	
	8	No-protocol mode	Protocol 4 mode	
	9	No-protocol mode ←→	No-protocol mode	
	A	Protocol 1 mode ←→	Protocol 1 mode	
	B	Protocol 2 mode ←→	Protocol 2 mode	
	C	Protocol 3 mode ←→	Protocol 3 mode	
	D	Protocol 4 mode ←→	Protocol 4 mode	
	E	Unavailable		
	F	Reserved for module test		

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